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30th International Symposium on Power Semiconductor Devices and ICs

May 13-17, 2018, Chicago, USA

PALMER HOUSE HILTON FLOOR DIRECTORY

Monday-Thursday registration and oral sessions (RED LACQUER). Wednesday banquet (GRAND BALLROOM).

Monday-Thursday coffee breaks, exhibition, poster sessions (SALON 4-9).

No ISPSD activities on this level.

Hotel check-in, Sunday registration and short course (HONORE ROOM), Monday reception (EMPIRE ROOM), bar and restaurants.

Arrival, coffee shops, restaurants, shops.

You can use the elevator or escalator to get to any of these floors. There are numerous restaurant and bar options both inside and outside the hotel. Please use www.yelp.com to find your choices.

SCHEDULE AT A GLANCE

Sun. May 13	Mon. May 14
Registration Desk 8:00-17:00 Honore Room (Lobby Level)	**Registration Desk** 7:00-17:00 Red Lacquer Room (4th Level)
Short Course 1: Silicon Charge Balance Devices 9:00-10:00 Honore Room (Lobby Level)	**Plenary 1** 8:30-10:20 Red Lacquer Room (4th Level)
Coffee Break 10:00-10:15	
Short Course 2: Device Loss Mechanisms 10:15-11:15	Coffee Break 10:20-10:40 Salon 4-9 (3rd Level)
Coffee Break 11:15-11:30	**Plenary 2** 10:40-12:10 Red Lacquer Room (4th Level)
Short Course 3: Sic Device Design & Fabrication 1:30-12:30	Lunch on Own 12:10-14:00
Lunch on Own 12:30-14:00	
Short Course 4: Vertical Gan Power Devices 14:00-15:00	**1. Superjunction MOS, Diodes and IGBTs** 14:00-15:40 Red Lacquer Room (4th Level)
Coffee Break 15:00-15:15	
Short Course 5: Algan/Gan Power Device Reliability 15:15-16:15	Coffee Break 15:40-16:00
Coffee Break 16:15-16:30	**2. SiC Power MOSFETs** 16:00-18:05 Red Lacquer Room (4th Level)
Short Course 6: Power Module Design and Assembly 16:30-17:30	
	Reception 18:15-20:15 (badge required) Empire Room (Lobby Level)

SCHEDULE AT A GLANCE

Tue. May 15	Wed. May 16	Thu. May 17
3. Lateral Devices: Reliability 8:30-10:10 Red Lacquer Room (4th Level)	**9. GaN Power Devices – 2** 8:30-10:10 Red Lacquer Room (4th Level)	**15. Novel Device Structures** 8:30-10:10 Red Lacquer Room (4th Level)
Coffee Break 10:10-10:30 Salon 4-9 (3rd Level)	Coffee Break 10:10-10:30 Salon 4-9 (3rd Level)	Coffee Break 10:10-10:30 Salon 4-9 (3rd Level)
4. Smart Power ICs 10:30-12:10 Red Lacquer Room (4th Level)	**Poster Sessions** **10. Low Voltage** **11. IC Design** **12. SiC** 10:30-12:10 Salon 4-9 (3rd Level)	**16. IGBTs** 10:30-12:10 Red Lacquer Room (4th Level)
Lunch on Own 12:10-13:30	Lunch on Own 12:10-13:30	Lunch on Own 12:10-13:30
5. GaN Power Devices – 1 13:30-15:10 Red Lacquer Room (4th Level)	**13. SiC Reliability and Ruggedness** 13:30-15:10 Red Lacquer Room (4th Level)	**17. Invited & Late News Papers** 13:30-15:10 Red Lacquer Room (4th Level)
Coffee Break 15:10-15:30 Salon 4-9 (3rd Level)	Coffee Break 15:10-15:30 Salon 4-9 (3rd Level)	**Closing** 15:10-15:40 Red Lacquer Room (4th Level)
Poster Sessions **6. High Voltage** **7. GaN** **8. Packaging** 15:30-17:10 Salon 4-9 (3rd Level)	**14. Packaging and Enabling Technologies** 15:30-17:35 Red Lacquer Room (4th Level)	
Ad Com Meeting/Dinner 18:30-21:30 (invitation only)	**Banquet** 18:30-21:30 (card required) Grand Ballroom (4th Level)	**TPC Dinner** 18:30-21:30 (invitation only)

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GENERAL CHAIR'S MESSAGE

It is my great honor and pleasure to welcome you on behalf of the Organizing Committee to the 30th IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD 2018) in the beautiful city of Chicago.

ISPSD2018 marks the 30th anniversary of ISPSD. Since its first meeting in Japan in 1988, ISPSD has become the world's premier forum for technical discussions in all areas of power semiconductor devices and power integrated circuits. The global power semiconductor industry has steadily grown into a $30 billion sector over the past three decades, enabling energy-efficient applications such as solar power, wind power, electric vehicles, ICT infrastructures, lighting and industrial drives. Over 1600 technical papers have been presented at ISPSD conferences. Most of the breakthrough power device technologies were first reported at ISPSD before they became phenomenal commercial successes. ISPSD2018 will celebrate 30 years of excellence in advancing power semiconductor technologies with a series of technical and social events during the conference. In particular, we will induct 32 distinguished colleagues into the newly established ISPSD Hall of Fame during the Wednesday 30th Anniversary Celebration Banquet. As a special celebration gift, we present you a complete collection of ISPSD proceedings 1988--2018 (including the two Electrochemical Society Workshops on High Voltage and Smart Power Devices and ICs in 1987 and 1989), thanks to the support of IEEE, IEEJ, ECS, and a group of dedicated volunteers.

Our plenary session on Monday will start with an opening keynote speech on "ISPSD: A 30 Year Journey in Advancing Power Semiconductor Technology" from three founding members of the conference, Drs. Ayman Shibib (USA), Leo Lorentz (Germany), and Hiromichi Ohashi (Japan), and followed by three other plenary speeches on "Silicon, GaN and SiC: There's Room for All" from Mr. Larry Spaziani, GaN Systems Inc., Canada, "Si Wafer Technology for Power Devices: A Review and Future Directions" from Mr. Norihisa Machida, SUMCO, Japan, and "The Future of Power Semiconductors: an EU Perspective" from Dr. Bert De Colvenaer, ECSEL, Belgium, respectively. We are extremely fortunate to have these distinguished leaders from industry to share their visions and wisdoms with us.

ISPSD2018 features 50 oral and 79 poster presentations on both silicon and WBG power devices which are selected from 245 abstracts from 23 countries/regions. On Sunday, we offer 6 short courses on a series of current and practical topics in the field.

Chicago is the third largest city in the United States, and an international hub for finance, commerce, industry, technology, telecommunications, and transportation. The city of Chicago is the birth

place of modern skyscrapers and a living museum of modern architecture. ISPSD 2018 is held in the historical Palmer House Hilton Hotel in the beautiful and safe downtown district ("Loop") of Chicago with numerous museums, parks, theaters, restaurants, and shops within a walking distance. We trust you and your family will enjoy your stay in Chicago. On Monday, we will host our Welcome Reception in the splendid Empire Room of the Palmer House. On Wednesday, we expect to see you all at the 30th Anniversary Celebration Banquet to enjoy Chicago jazz/blues music, wines and delicious meals. Our family and companion programs offer exciting city tours on Monday, and Tuesday, and Wednesday.

We are pleased to acknowledge the support of our Gold Partners PowerAmerica and Sinopower Semiconductor, and Silver Partners Applied Materials, ShinDengen, Synopsys, and Tektronix. Their support and participation have created a very strong industrial relevance. We will have 17 exhibitors in the exhibition/coffee area (Salon 4-9 on the 3rd Floor) Monday through Thursday. The exhibitors will showcase their state-of-the-art technologies, products, and solutions, creating a highly interactive networking environment when mixing with the poster sessions and coffee breaks in the same space.

I would like to express my utmost gratitude to the members of the organizing committee, the technical program committee, and the advisory committee, who with hard work and selfless dedication have made this conference possible. I wanted to thank each and every one of you as a presenter, an attendee, an exhibitor, a volunteer, or any combined role of the above for your contribution and participation.

Once again I welcome you to ISPSD2018. Together we help deliver a more sustainable future.

Z. John Shen, General Chair

ORGANIZATION

ORGANIZING COMMITTEE

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GENERAL INFORMATION

Conference Venue

Palmer House Hilton
17 E Monroe St, Chicago, IL 60603
+1 (312) 726-7500

Conference discount room rates are available via www.ispsd2018.com until April 13, 2018. Please use the floor directory on Page 2 for detailed meeting room information.

Conference Registration

In order to participate in the ISPSD2018 conference, you must register online for the conference at www.ispsd2018.com using your credit card. You need to wear your badge in all conference activities. The conference reception desk hour/location information is as the following:

Sunday, May 13	8:00-17:00	Honore Room, Lobby Level
Monday, May 14	7:00-17:00	Red Lacquer Room, 4th Level
Tuesday, May 15	8:00-17:00	Red Lacquer Room, 4th Level
Wednesday, May 16	8:00-17:00	Red Lacquer Room, 4th Level
Thursday, May 17	8:00-13:00	Red Lacquer Room, 4th Level

Registration Fees

Early fees apply to registration applications completed by April 15, 2018.

	Early Fee	Late Fee
IEEE/IEEJ Member	$650	$800
Non-Member	$750	$900
Student IEEE Member	$350	$450
Student Non-Member	$450	$500
Short Course IEEE/IEEJ Member	$400	$500
Short Course Non-Member	$500	$600
Short Course Student IEEE Member	$200	$250
Short Course Student Non-Member	$250	$300

Cancellation and Refund Policy for Completed Registrations

Conference registration cancellation requests made via email. Requests made before April 30, 2018 will be processed with a fee of $75, after April 30, 2018 will be processed with a fee of $200. Request made after May 13, 2018 will not be processed.

Short course registration cancellation requests made via email. Requests made before May 12, 2018 will be processed with a fee of $50. Requests made after May 12, 2018 will not be processed.

Local Transportation

Chicago-O'Hare International Airport

Distance from hotel:	29km (18 mi)
Travel time:	50 min
Cost:	$5

Directions: We recommend taking the subway Blue Line from O'Hare International Airport (ORD) to Monroe Station. Palmer House Hilton is 3 minute walk from Monroe Station. This is the cheapest and often quickest way to get to the hotel from ORD.

If coming from domestic or international flights arriving at Terminals 1, 2 or 3, follow the signs in the airport to "CTA Trains" or "Trains to City." The train station is less than 10 minute walk from baggage claim in each of these 3 terminals. If arriving at International Terminal 5, follow the signs to the Airport Transit System (ATS). Ride the train to Terminal 2, then follow signs to "CTA Trains" or "Trains to City." Once at the Terminal 2 train station, use the vending machine to purchase a single-ride or multi-day card (Ventra Card).

For more information on the subway service ("the L"), please visit http://www.transitchicago.com/airports/.

Chicago Midway Airport

Distance from hotel:	19km (12 mi)
Travel time:	30 min
Cost:	$2.45

Directions: We recommend taking the subway Orange Line from Midway International Airport (MDW) to Adams/Wabash Station. Palmer House Hilton is 3 minute walk from Adams/Wabash station. This is the cheapest and often quickest way to get to the hotel from MDW.

At the airport, simply follow the sign "CTA Trains" or "Trains to City" from the MDW terminal and use the vending machine at the train station to purchase a single-ride or multi-day card (Ventra Card). For more information on the subway service ("the L"), please visit www.transitchicago.com/airports/.

Alternate Options: You can also use a taxi or Uber service. The cost from ORD to the hotel is around $40-$60 and the travel time is between 40 and 60 minutes. The cost from MDW to the hotel is around $20-$30 and the travel time is between 20 and 40 minutes. We do not recommend renting a car due to the very high parking cost and traffic congestion in the city.

Instruction for Oral Presentation

Each oral presentation is allocated 25 minutes, including 5 minutes for Q&A. We must use the on-site laptop PC in the session room for oral presentations (OS: Windows7, PowerPoint 2007 / 2010 / 2013 /

2016, and pdf format files are acceptable). The screen format is 4:3 and projector resolution is XGA (1024 x 768 pixel). Organizer cannot guarantee the quality of Macintosh-based presentations, so check in advance their Windows compatibility. Please bring your data USB to the operation desk in the front row of the conference room at least 30 minutes before the beginning of your session. Please meet with your session chairs at least 20 minutes prior to the start of your presentation, and be seated at the "Next Speaker's seat" located in the front row. Please contact the registration desk in case you need assistance.

Instruction for Poster Presentation

Your poster should be no larger than 4' x 4' (1.2m x 1.2m) in size. Your poster should be displayed on the assigned board by paper ID using pushpins (available at the poster room). No other adhesive material is permitted on the boards. Please set up your poster one hour before the start of your poster session (see the program schedule). You are responsible for removing the poster after the session. You are expected to be in front of your poster throughout the session to answer questions.

Recording and Photography Policy

IEEE policy prohibits video recording or photographing of presentations unless permission from the presenter is obtained in advance. Photographing of people or social events is permitted.

Monday Welcome Reception

18:15-20:15 Monday May 14 in the Empire Room on Lobby Level.

Please join us for wine, beer, and snacks, catch up with old friends and make a few new friends. Please use your conference badge to participate (no separate ticket is required).

Wednesday 30th Celebration Banquet

18:30-21:00 Wednesday, May 16 in Grand Ballroom on 4th Level.

Please join us to celebrate the 30th anniversary of ISPSD in a Chicago themed banquet with jazz/blues performance. 32 distinguished colleagues will be inducted into the newly established ISPSD Hall of Fame. You will need to use the special invitation card to enter the banquet.

The main entrée will be a combo dish of beef and sea scallop. Alternative options (vegetarian only, beef only, scallop only) can be arranged ONLY if you check with the registration desk when you check-in. Please also inform us during check-in if you do NOT plan to attend the banquet. This will help us better plan the banquet seating.

Coffee Breaks, Poster Sessions, and Exhibition

Monday through Thursday in Salon 4-9 on 3rd Level (one level below our main meeting room).

We use the Salon space to relax, network, and stop by the tabletop exhibition during coffee breaks and the poster sessions. You can use escalator or elevator to move between the main meeting room (Red Lacquer on 4th Level) and the Salon.

Spouse and Guest Program

ISPSD2018 is glad to organize the following tours and activities (tentatively) for families and guests. Please encourage your guest to stop by the hospitality desk in the registration area to check out the final schedule and make reservation:

Chicago Architecture Foundation River Cruise Tour: Estimated cost: $40 per person. Estimated tour time: 2 hours, tentatively scheduled for Monday

Chicago Architecture Walking Tour: Estimated cost: $20 per person. Estimated tour time: 2 hours, tentatively scheduled for Tuesday

Art Institute Chicago: Estimated cost: $25 per person.
Estimated tour time: 2-5 hours, tentatively scheduled for Wednesday

In addition, the following links provide best ways to tour the city on your own:

- Citypass: www.citypass.com/chicago
- Hop-on-hop-off bus: www.bigbustours.com/en/chicago/chicago-bus-tours/

ISPSD HALL OF FAME

The purpose of the ISPSD Hall of Fame (IHF) is to honor individuals who have made high impact contributions in advancing power semiconductor technology and/or in sustaining the success of ISPSD. Starting this year, the IHF replaces the traditional "Contributory Awards" and "Pioneer Awards". The AdCom has selected the following 32 distinguished colleagues as the first inductees into the ISPSD Hall of Fame:

Michael S. Adler	for contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences
G.A.J. Amaratunga	for contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences
B. Jayant Baliga	for contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences
Xingbi Chen	for contributions to superjunction power semiconductor devices
Tat-Sing Paul Chow	for contributions to silicon and wide bandgap power semiconductor devices, and his leadership role in organizing ISPSD conferences
Mohamed Darwish	for contributions to the advancement of power semiconductor technology, and his leadership role in organizing ISPSD conferences
Taylor R. Efland	for contributions to power IC technology, and his leadership role in organizing ISPSD conferences
Wolfgang Fichtner	for contributions to MOS gated thyristors and TCAD modeling tools, and his leadership role in organizing ISPSD conferences
Min-Koo Han	for contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences
Phil Hower	for contributions to power device safe operating area study and power IC technology
A. A. Jaecklin	for contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Daniel Kinzer	for contributions to power MOSFET technology, and his leadership role in organizing ISPSD conferences
Leo Lorenz	for contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences
Gourab Majumdar	for contributions to IGBT and intelligent power module technology, and his leadership role in organizing ISPSD conferences
Jose Millan	for contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences
Peter Moens	for contributions to integrated power technology and GaN power device and reliability, and his leadership role in organizing ISPSD conferences
Akio Nakagawa	for contributions to IGBT and power IC technology
Hiromichi Ohashi	for contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences
Tadahiro Ohmi	for contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences
Masahiro Okamura	for contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences
James Plummer	for contributions to MOS-bipolar power devices and power ICs, and for inspiring and training a new generation of device researchers
C. A. T. Salama	for contributions to power IC technology, and his leadership role in organizing ISPSD conferences
Yasukazu Seki	for contributions to IGBT technology, and his leadership role in organizing ISPSD conferences
M. A. Shibib	for contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Dieter Silber	for contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences
Paolo Spirito	for contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences
Yoshitaka Sugawara	for contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences
Yoshiyuki Uchida	for contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences
Harry Vaes	for contributions to RESURF technology
Carl F. Wheatley	for contributions to IGBT and radiation-hard power device technology
Richard K. Williams	for contributions to trench power MOSFET and power IC technology, and his leadership role in organizing ISPSD conferences
Toshiaki Yachi	for contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Deceased members in BOLD

AWARDS

THE OHMI BEST PAPER AWARD

The Best Paper Award was renamed to "The Ohmi Best Paper Award" in honor of the late Prof. Ohmi's outstanding contributions to the ISPSD. The Ohmi Best Paper Award will be granted to the author(s) of a paper determined to be the best overall in the ISPSD2018.

ISPSD2017 THE OHMI BEST PAPER AWARD
A Novel Hybrid Power Module with Dual Side-Gate HiGT and SiC-SBD

Abstract: In this paper, a novel hybrid power module using a new combination of dual side-gate HiGTs (high-conductivity IGBT) and SiC-SBDs is proposed. This combination achieves drastic switching loss reductions at a turn-off loss of −43%, a turn-on loss of −71%, and a reverse recovery loss of −98% compared with a conventional combination of trench gate HiGTs and U-SFDs (ultra soft & fast recovery diode). As a result, the proposed DuSH module (dual side-gate HiGT hybrid module) has an extremely low inverter loss of −50%, similar to SiC-MOSFETs.

Yujiro Takeuchi received the B.S. and M.S. degrees in maritime science from Kobe University, Hyogo-ken, Japan in 2010 and 2012. He joined Hitachi, Ltd., Ibaraki-ken, Japan, in 2012, where he has been engaged in research on power semiconductor devices.

Tomoyuki Miyoshi received the B.S., M.S., and Ph.D. in Tohoku University, Miyagi, Japan, in 2005, 2007, and 2015. In 2007, he joined Hitachi, Ltd., Japan. He is currently engaged in research and development of power device technologies.

Tomoyasu Furukawa received the B.S. and M.S. degrees in Hiroshima University in 2000 and 2002. He joined Hitachi, Ltd, Japan, in 2002. He is currently engaged in research and development of power device technologies.

Masaki Shiraishi received the B.S. and M.S. degrees in Tokyo Institute of Technology in 1996 and 1998. He joined Hitachi, Ltd, Japan, in 1998. He has been engaged in research and development of power semiconductor devices.

Mutsuhiro Mori received the B.E., M.E. and Ph. D. degrees in science and engineering from Waseda University, Tokyo, Japan. Since 1979, he has been with the Hitachi Research Laboratory, Hitachi, Ltd. He has been engaged in the research and development of optimal energy saving control systems with IT and power semiconductor devices, such as the light-triggered thyristors, GaAs power static induction transistors (SIT), one chip inverter ICs, high-voltage driver ICs, soft and fast recovery diodes (SFD), and high-conductivity insulated gate bipolar transistors (HiGT). He is a member of the Institute of Electrical Engineers of Japan (IEEJ) and a senior member of the Institute of Electrical and Electronics Engineers (IEEE).

CHARITAT AWARD
(YOUNG RESEARCHER AWARD)

A young researcher (age less than 30 at the time of the conference) who is both first author and presenter of a paper will be nominated to the award.

The Charitat award will be presented during the closing ceremony of the conference. The Ohmi best paper award will be presented during the ISPSD2019 opening session.

ISPSD 2017 CHARITAT AWARD
High Performance Fully-Recessed Enhancement-Mode GaN MIS-FET with Crystalline Oxide Interlayer

Abstract: In this work, we developed an effective technique to form a sharp and stable crystalline oxidation interlayer (COIL) between the reliable LPCVD (low pressure chemical vapor deposition)-SiN_x gate dielectric and recess-etched GaN channel. The COIL was formed using oxygen-plasma treatment, followed by *in-situ* annealing prior to the LPCVD-SiN_x deposition. The COIL plays the critical role of protecting the etched GaN surface from degradation during high-temperature (i.e. at ~ 780 ^{o}C) process, which is essential for fabricating enhancement-mode GaN MIS-FETs with highly reliable LPCVD-SiN_x gate dielectric and fully recessed gate structure. The LPCVD-SiN_x/GaN MIS-FETs with COIL deliver normally-off operation with a V_{TH} of 1.15 V, small on resistance, thermally stable V_{TH} and low positive-bias temperature instability (PBTI).

Mengyuan Hua received the B.S. degree in Physics from Tsinghua University, Beijing, China, in 2013. She then joined the Hong Kong University of Science and Technology (HKUST), Hong Kong, China, where she received the Ph.D. degree in Electronic and Computer Engineering in 2017 under the supervision of Prof. Kevin J. Chen. Currently, she is a research associate at HKUST. Her research interests include GaN-based power device technology and device reliability.

PL1-1: ISPSD: A 30 Year Journey in Advancing Power Semiconductor Technology

Ayman Shibib, *Vishay Siliconix, United States;* Leo Lorenz, *ECPE/ Infineon, Germany;* Hiromichi Ohashi, *NEPRC-J, Japan*

Abstract: Celebrating the 30th Anniversary of ISPSD is a very special occasion to reflect on the origin and roots of the conference and how it came about to be the premier international conference on Power Semiconductor Devices and ICs. A review of the events that led to its formation and development is presented. Another aspect of this celebration is the review of the contributions of ISPSD to the Power Device technical community covering wide and diverse power device areas and applications throughout the 30 years history of ISPSD. The future prospects of Power Devices and ISPSD in the next years is briefly mentioned.

PL1-2: Silicon, GaN and SiC: There's Room for All – An Application Space Overview of Device Considerations

Larry Spaziani, Lucas Lu, *GaN Systems, Canada*

Abstract: The discrete power device marketplace is estimated between 15 and 22 billion dollars and is comprised primarily of transistors and diodes in a variety of voltage, current, packaging and power ratings. It is an area of intense focus as new technologies such as wide bandgap emerge and new applications such as electric vehicles emerge. Decision makers from Engineers to CEO's are faced with the same decisions they have always faced, comparing power, efficiency and size, yet the decisions are more difficult given the fast-moving pace of these emerging technologies. In this paper, several application spaces ranging from consumer to vehicle to motors will be reviewed, comparing the most critical aspects of the applications against semiconductor choices these decision makes have available. Considerations of the appropriate technologies will be reviewed comparing where the technologies have been, are today, and where they will be in the next 5 years.

PL2-1: Si Wafer Technology for Power Devices: A Review and Future Directions

Norihisa Machida, *SUMCO Corporation, Japan*

Abstract: Silicon wafers have been widely used in semiconductor devices for years. Their characteristics have been improved by untiring development efforts to meet power device manufacturers' requirements such as lowering substrate resistivity for Power MOSFET and reducing resistivity variation for IGBT. As future directions, by utilizing advantages of silicon wafers, adoption of MCZ

grown bulk silicon wafers for low and middle voltage IGBT and introduction of 300mm size silicon wafers will proceed.

PL2-2: The Future of Power Semiconductors: An EU Perspecitve
Bert De Colvenaer, *ECSEL JU, Belgium*

Abstract: With the integration of more renewable energy sources (RES) in the European landscape, with more stringent demands on supply and with cost conscious customers, and also environmental conscious, Europe calls for a smarter energy landscape where power semiconductors will play a major role in the years to come.

SHORT COURSE

The short course this year is supported by Sinopower Semiconductor and other industrial partners.

Time	Title	Speaker
09:00-10:00	Advances in Silicon Power Technology	Madhur Bobde
10:00-10:15	Coffee Break	
10:15-11:15	Perspective of Loss Mechanisms in Silicon and Wide Bandgap Power Devices	Gerald Deboy
11:15-11:30	Coffee Break	
11:30-12:30	Silicon Carbide Power Device Design and Fabrication: Making the Transition from Silicon	Victor Veliadis
12:30-14:00	Lunch Break	
14:00-15:00	Vertical GaN Power Devices	Isik C. Kizilyalli
15:00-15:15	Coffee Break	
15:15-16:15	AlGaN/GaN Power Device Reliability	Peter Moens
16:15-16:30	Coffee Break	
16:30-17:30	Multi-Chip Semiconductor Power Module Design and Assembly: Rethinking Established Packaging Solutions for Improved Performance, Robustness and Reliability	A. Castellazzi

SC1. Advances in Silicon Power Technology

Madhur Bodge, *Alpha & Omega Semiconductor*

Abstract: Silicon power MOSFETs have made tremendous advancements in the past decade. The key concept that has led to this is that of charge balance. In conventional power MOSFET device the maximum doping level and the thickness of the drift region is limited by blocking voltage constraints and a triangular electric field results in its sub-optimal utilization.

The concept of charge balance involves adding an opposite polarity of charge in the drift region compared to default doping to modify the shape of electric field from triangular to trapezoidal for better utilization of drift region for voltage blocking and allow significantly higher doping concentration for lower conduction losses. For low voltages (below 400V) the popular device structure to achieve this is the Split Gate Transistor (SGT). This device utilizes trench MOS charge balance with a shield electrode under the gate. In addition to significantly improving the On Resistance per unit area (~3x for 100V blocking), the shield electrode also significantly reduced the gate to drain miller capacitance (Crss) and Crss/Ciss ratio to allow for high frequency switching.

For high voltages above 400V, the depth of trench and thickness of liner oxide make SGT device impractical to fabricate. As a result, the Super-Junction transistor has emerged as the most successful MOSFET for high voltages. This device utilizes alternating P and N columns in the drift region thereby creating a charge balance. Methods such as multi epi, deep trench and fill have been demonstrated and are commercially successful for making superjunction transistors. These can achieve an On-Resistance reduction of up to 8x compared to planar DMOS transistor. However, presence of alternating P and N columns also results in peculiar Capacitance curves, particularly the Crss which drops sharply at low drain biases and then increases at higher drain biases. It also exhibits snappy diode reverse recovery.

Charge balanced structure is also finding use in bipolar devices such as IGBT and Fast recovery diodes. In these devices, charge balance is used for various performance enhancements such as improving turn-off losses, injection enhancement, and controlling injection efficiency for faster switching.

The goal of this seminar is to understand the device physics and electrical characteristics of charge balanced devices in unipolar and bipolar power devices. This seminar is intended for intermediate level audience.

SC2. Perspective of Loss Mechanisms in Silicon and Wide Bandgap Power Devices

Dr. Gerald Deboy, *Infineon Technologies Austria AG*

Abstract: This short course will discuss switching losses for power semiconductor devices from a physical device point of view. The focus will be laid on power MOSFETs based on Superjunction technology and GaN high electron mobility transistors as two prominent examples of the silicon and the wide bandgap world. We will give a perspective of loss mechanisms in the light of recent developments of the two fundamental device concepts.

Based on these loss mechanisms appropriate circuits and control methods are discussed yielding best efficiency for both device concepts respectively.

The short course addresses researchers interested in a deep understanding of the device properties as well as users of modern power semiconductor devices seeking best matching between topology, control and power device.

SC3. Silicon Carbide Power Device Design and Fabrication: Making the Transition from Silicon

Victor Veliadis, PhD, *Deputy Executive Director and CTO, PowerAmerica*

Abstract: The tutorial will outline the advantages of SiC over other power electronic materials, and will introduce SiC devices currently developed for power electronic applications. ESD, high-voltage testing, and packaging aspects will be covered. The design and properties of SiC JFETs, MOSFETs, BJTs, IGBTs, Thyristors, and Junction Barrier Schottky and PiN diodes will be discussed, with an emphasis on their performance advantages over those of their Si counterparts. Common SiC Edge Termination techniques, which allow SiC devices to exploit their full high-voltage potential, will be rigorously treated and their impact on device performance will be highlighted. Aspects of device fabrication will be taught with an emphasis on the processes that do not carry over from the mature Si manufacturing world and are thus tailored to SiC. In particular, the tutorial will stress in more detail the design and fabrication of SiC MOSFETs, which are being inserted in the majority of SiC based power electronic systems. Device reliability will be reported through exemplary hard switching results. Exemplary SiC-based power electronics systems like hybrid loaders, fast chargers, PV inverters, EV traction, and circuit breakers will highlight the significant advantages of these systems over their Silicon based counterparts.

This tutorial is intended for intermediate level audiences.

SC4. Vertical Power Electronic Devices based on Bulk GaN Substrates

Dr. Isik C. Kizilyalli, *Program Director at the Advanced Research Projects Agency – Energy (ARPA-E), Department of Energy*

Abstract: Silicon (Si) has been the semiconductor material of choice for power devices for quite some time due to cost, ease of processing, and the vast amount of information available about its material properties. Si devices are, however, reaching their operational limits in blocking voltage capability, operation temperature, and switching frequency due to the intrinsic material properties of Si. Wide bandgap (WBG) power semiconductors, such as gallium nitride (GaN) and silicon carbide (SiC), are an attractive emerging alternative to Si in many applications. Power converters based on WBG devices can achieve both higher efficiency and higher gravimetric and volumetric power conversion densities than the equivalent Si based converters. The power figure of merit (PFOM), which captures the trade-off between the device specific resistance (Rsp) versus the device BV clearly illustrates the advantage of GaN over Si and SiC devices. This arises from the cubed dependence of the figure-of-merit on the critical electric field where the critical electric field for GaN is 10 times that of Si and 1.6 times that of SiC. To date, the majority of GaN power device development has been directed toward lateral architectures, such as high-electron mobility transistors (HEMTs), fabricated in thin layers of GaN grown on foreign substrates (including Si or SiC). Such lateral devices suffer from well-known issues such as current-collapse, dynamic on-resistance, inability to support avalanche breakdown, and inefficient thermal management. Many of these shortcomings arise from defects originating in the very large lattice and coefficient of thermal expansion (CTE) mismatch between GaN and the substrate. Furthermore, most power electronics semiconductor and diodes are vertical architectures. Fabricating vertical semiconductor device structures on lattice and CTE matched bulk GaN substrates possible to realize the material-limited potential of GaN including true avalanche-limited breakdown and more efficient thermal management, leading to large device currents (> 100A) without resorting to device parallelization, high breakdown voltages (1.2 to 5kV), and increased number of die on a wafer. Recent availability of both 2- and 4-inch bulk GaN substrates is enabling breakthroughs in GaN device performance with vertical diode structures. In this tutorial recent advances in bulk GaN substrates and vertical architecture GaN power electronic devices (diodes, transistors, and application circuits) is surveyed with emphasis on the ARPA-E (Department of Energy) funded projects in the SWITCHES and PNDIODES Programs along with recent significant advances made in Japan. The SWITCHES Program (launched 2013) aimed to catalyze the development of vertical GaN devices using innovations in materials and/or device architectures that drive the costs of the devices. The goal was to enable the development of high voltage (>1200V), high current (100A) single die power semiconductor devices that, upon

ultimately reaching scale, would have the potential to reach functional cost parity with Si power transistors while also offering breakthrough relative circuit performance (low losses, high switching frequencies, and high temperature operation). The PNDIODES (Power Nitride Doping Innovation Offers Devices Enabling SWITCHES, launched 2017) Program funds transformational advances and mechanistic understanding in the process of selective area doping in the III-Nitride wide band gap (WBG) semiconductor material system and the demonstration of arbitrarily placed, reliable, contactable, and generally useable p-n junction regions that addresses a major obstacle, enables high- performance and reliable GaN vertical power electronic semiconductor devices.

SC5. AlGaN/GaN Power Device Reliability

Dr. Peter Moens, *ON Semiconductor Belgium*

Abstract: AlGaN/GaN power devices have made tremendous progress over the past few years, and first commercial products have entered the market. The quality of MOCVD has reached a level that allows the fabrication of large area transistors with high yield and good reproducibility. Although GaN power devices achieve substantial higher system efficiency compared to their Si counterparts, the widespread adoption of GaN power devices in the market is still hampered by the unknown field reliability.

The tutorial will focus on the current understanding of the different intrinsic and extrinsic reliability mechanisms of AlGaN GaN power devices, and will cover following aspects:

- A methodology on how to extract important information on the conduction mechanisms in the GaN buffer structure out of relatively simple measurements on TLM structures (back-gating or substrate ramp) and transistors (current DLTS).
- Overview of the main intrinsic reliability mechanisms: gate reliability (both MISHEMT and pGaN gate), NBTI/PBTI of MISHEMTs, accelerated drain stress and hot carrier stress (semi-on-state stress). Recoverable versus permanent degradation.
- GaN-specific failure and degradation modes such as the inverse piezo-electric effect and dynamic Ron.
- Acceleration models and statistical distribution models (Weibull, lognormal) applied to GaN.
- Extrinsic reliability (HTRB, HTGB, thermal cycling etc).
- Switching reliability (double pulse testing, boost converter, ...)
- Introduction to the new upcoming JEDEC standard for AlGaN/GaN power devices (JC 70.1).

The topic will be treated in-depth and is for an intermediate-advanced audience.

SC6. Multi-Chip Semiconductor Power Module Design and Assembly: Rethinking Established Packaging Solutions for Improved Performance, Robustness and Reliability

Dr. Alberto Castellazzi, *Associate Professor of Power Electronics, Power Electronics, Machines and Control Group University of Nottingham*

Abstract: This short-course analyses the typical structure and assembly process of commercial power modules. Based on real application examples, it goes on to illustrate key operational electro- thermal and thermo-mechanical effects which prevent the achievement of disruptive efficiency, power density, robustness and reliability. It then presents innovative concepts and design approaches enabling progress beyond state-of-the-art and discusses the transfer of technology to new and upcoming wide-band-gap semiconductor technologies. In closing, package bespoke design methodologies and tools are addressed, with a focus on future virtual prototyping needs to support competitive development of increasingly integrated solutions.

The course targets an audience with entry to intermediate level knowledge of power device packaging; the topic is treated in general at the survey level, with some punctual aspects only dealt more in depth.

Opening Remarks
Red Lacquer Room (4th Level)
08:30 **Monday, May 14, 2018**
John Shen, *Illinois Institute of Technology, USA*

08:50 **Plenary 1**
Red Lacquer Room (4th Level)
Monday, May 14, 2018
Chair: John Shen, *Illinois Institute of Technology, USA*
Co-chair Kuang Sheng, *Zhejiang University, China*

08:50 **PL1-1** **ISPSD: 30 Year Journey in Advancing Power Semiconductor Technology**
Ayman Shibib, *Vishay Siliconix, United States;*
Leo Lorenz, *ECPE/Infineon, Germany;*
Hiromichi Ohashi, *NEPRC-J, Japan*

09:35 **PL1-2** **Silicon, GaN and SiC: There's Room for All – An Application Space Overview of Device Considerations**
Larry Spaziani, Lucas Lu, *GaN Systems, Canada*

10:20 **Coffee Break**
Salon 4-9 (3rd Level)
Monday, May 14, 2018

Plenary 2
Red Lacquer Room (4th Level)
Monday, May 14, 2018
Chair: Wai Tung Ng, *University of Toronto, Canada*
Co-chair Kevin Chen, *Hong Kong University of Science and Technology, China*

10:40 **PL2-1** **Si Wafer Technology for Power Devices: A Review and Future Directions**
Norihisa Machida, *SUMCO Corporation, Japan*

11:25 **PL2-2** **The Future of Power Semiconductors: An EU Perspecitve**
Bert De Colvenaer, *ECSEL JU, Belgium*

12:10 **Lunch Break**
Monday, May 14, 2018

1. Superjunction MOS, Diodes and IGBTs

Red Lacquer Room (4th Level)
Monday, May 14, 2018
Chair: Young Chul Choi, *ON Semiconductor, Korea*
Co-chair Marina Antoniou, *University of Cambridge, UK*

14:00 **1-1** **IGBT with Superior Long-Term Switching Behavior by Asymmetric Trench Oxide**
C. Sandow, P. Brandt, H.-P. Felsl, F.-J. Niedernostheide, F. Pfirsch, H.-J. Schulze, A. Stegner, F. Umbach, *Infineon Technologies AG, Germany;* F. Santos, W. Wagner, *Infineon Technologies Austria AG, Austria*

14:25 **1-2** **6.5 kV Field Shielded Anode (FSA) Diode Concept with 150C Maximum Operational Temperature Capability**
B.K. Boksteen, C. Papadopoulos, D. Prindle, A. Kopta, C. Corvasce, *ABB Switzerland Ltd., Switzerland*

14:50 **1-3** **Low Noise Superjunction MOSFET with Integrated Snubber Structure**
Hiroaki Yamashita, Syotaro Ono, Hisao Ichijo, Masataka Tsuji, *Toshiba Electronic Devices & Storage Corporation, Japan;* Takenori Yasuzumi, *Toshiba Corporation, Japan;* Masaru Izumisawa, Wataru Saito, *Toshiba Electronic Devices & Storage Corporation, Japan*

15:15 **1-4** **Breakthrough of Drain Current Capability and On-Resistance Limits by Gate-Connected Superjunction MOSFET**
Wataru Saito, *Toshiba Electronic Devices & Storage Corporation, Japan*

15:40 **Coffee Break**
Salon 4-9 (3rd Level)
Monday, May 14, 2018

2. SiC Power MOSFETs

Monday, May 14, 2018
Red Lacquer Room (4th Level)
Chair: Peter Losee, *General Electric, USA*
Co-chair Andrei Petru Mihaila, *ABB, Switzerland*

16:00 **2-1** **Investigation of Threshold Voltage Stability of SiC MOSFETs**
Dethard Peters, *Infineon Technologies AG, Germany,* Thomas Aichinger, *Infineon Technologies Austria AG, Austria,* Thomas Basler, *Infineon Technologies AG, Germany,* Gerald Rescher, *Infineon Technologies Austria AG, Austria,* Katja Puschkarsky, Hans Reisinger, *Infineon Technologies AG, Germany*

16:25 **2-2** **Deep-P Encapsulated 4H-SiC Trench MOSFETs with Ultra Low $R_{on}Q_{gd}$**
Yasuhiro Ebihara, Aiko Ichimura, Shuhei Mitani, Masato Noborio, Yuichi Takeuchi, Shoji Mizuno, Toshimasa Yamamoto, Kazuhiro Tsuruta, *Denso Corporation, Japan*

16:50 **2-3** **Influence of the Off-State Gate-Source Voltage on the Transient Drain Current Response of SiC MOSFETs**
Christian Unger, Martin Pfost, *Technische Universität Dortmund, Germany*

17:15 **2-4** **Reduction of RonA Retaining High Threshold Voltage in SiC DioMOS by Improved Channel Design**
Atsushi Ohoka, Masao Uchida, Tsutomu Kiyosawa, Nobuyuki Horikawa, Kouichi Saitou, Yoshihiko Kanzawa, Haruyuki Sorada, Kazuyuki Sawada, Tetsuzo Ueda, *Panasonic Corporation, Japan*

17:40 **2-5** **Avalanche Ruggedness and Reverse-Bias Reliability of SiC MOSFET with Integrated Junction Barrier Controlled Schottky Rectifier**
Cheng-Tyng Yen, Fu-Jen Hsu, Chien-Chung Hung, Chwan-Ying Lee, Lurng-Shehng Lee, Ya-Fang Li, Kuo-Ting Chu, *Hestia Power Inc., Taiwan*

Reception

Empire Room (Lobby Level)

18:15 **Monday, May 14, 2018**

3. Lateral Devices: Reliability

Red Lacquer Room (4th Level)

Tuesday, May 15, 2018

Chair: Phil Rutter, *Nexperia, UK*

Co-chair Jun Cai, *Texas Instruments, USA*

08:30 **3-1** **Comprehensive Investigation on Mechanical Strain Induced Performance Boosts in LDMOS**
Wangran Wu, Siyang Liu, Jing Zhu, Weifeng Sun, *Southeast University, China*

08:55 **3-2** **Investigation on Total-Ionizing-Dose Radiation Response for High Voltage Ultra-Thin Layer SOI LDMOS**
Xin Zhou, Lingfang Zhang, Ming Qiao, Zhangyi'an Yuan, Ping Luo, *University of Electronic Science and Technology of China, China;* Lei Shu, *Harbin Institute of Technology, China;* Zhaoji Li, Bo Zhang, *University of Electronic Science and Technology of China, China*

09:20 **3-3** **Electromigration Current Limit Relaxation for Power Device Interconnects**
Jungwoo Joh, Young-Joon Park, Srikanth Krishnan, Kim Christensen, Jayhoon Chung, *Texas Instruments, United States*

09:45 **3-4** **Performance and Reliability Insights of Drain Extended FinFET Devices for High Voltage SoC Applications**
B. Sampath Kumar, Milova Paul, Mayank Shrivastava, *Indian Institute of Science, India;* Harald Gossner, *Intel Deutschland GmbH, Germany*

10:10 **Coffee Break**
Salon 4-9 (3rd Level)
Tuesday, May 15, 2018

4. Smart Power ICs

Red Lacquer Room (4th Level)
Tuesday, May 15, 2018
Chair: Nicolas Rouger, *CNRS, France*
Co-chair Budong (Albert) You, *Silergy Corp., China*

10:30 **4-1** **High-Speed, High-Reliability GaN Power Device with Integrated Gate Driver**
Gaofei Tang, *Hong Kong University of Science and Technology, China;* M.-H. Kwan, *Taiwan Semiconductor Manufacturing Company Limited, Taiwan;* Zhaofu Zhang, Jiabei He, Jiacheng Lei, *Hong Kong University of Science and Technology, China;* R.-Y. Su, F.-W. Yao, Y.-M. Lin, J.-L. Yu, Thomas Yang, Chan-Hong Chern, Tom Tsai, H.C. Tuan, Alexander Kalnitsky, *Taiwan Semiconductor Manufacturing Company Limited, Taiwan;* Kevin J. Chen, *Hong Kong University of Science and Technology, China*

10:55 **4-2** **A 600V High-Side Gate Drive Circuit with Ultra-Low Propagation Delay for Enhancement Mode GaN Devices**
Yangyang Lu, Jing Zhu, Weifeng Sun, *Southeast University, China;* Yunwu Zhang, *Southeast University and China Resources Microelectronics Limited, China;* Kongsheng Hu, Zhicheng Yu, Jing Leng, *Southeast University, China;* Shikang Cheng, Sen Zhang, *CSMC Technologies Corporation, China*

11:20 **4-3** **A Smart Gate Driver IC for GaN Power Transistors**
Jingshu Yu, Wei Jia Zhang, Andrew Shorten, Rophina Li, Wai Tung Ng, *University of Toronto, Canada*

11:45 **4-4** **[Late News] CMOS Bi-Directional Ultra-Wideband Galvanically Isolated Die-to-Die Communication Utilizing a Double-Isolated Transformer**
Mahdi Javid, *Arizona State University, United States;* Karel Ptacek, *ON Semiconductor, Czech Republic;* Richard Burton, *Atomera Inc., United States;* Jennifer Kitchen, *Arizona State University, United States*

12:10 **Lunch Break**

Tuesday, May 15, 2018

5. GaN Power Devices - 1

Red Lacquer Room (4th Level)

Tuesday, May 15, 2018

Chair: Kevin Chen, *Hong Kong University of Science and Technology, China*

Co-chair Oliver Haeberlen, *Infineon Technologies, Austria*

13:30 **5-1** **Dynamic-Ron Control via Proton Irradiation in AlGaN/GaN Transistors**
A. Tajalli, *Università degli Studi di Padova, Italy;* A. Stockman, *ON Semiconductor, CMST imec/Ghent University, Belgium;* M. Meneghini, *Università degli Studi di Padova, Italy;* S. Mouhoubi, A. Banerjee, *ON Semiconductor, Belgium;* S. Gerardin, M. Bagatin, A. Paccagnella, E. Zanoni, *Università degli Studi di Padova, Italy;* M. Tack, *ON Semiconductor, Belgium;* B. Bakeroot, *CMST imec/Ghent University, Belgium;* P. Moens, *ON Semiconductor, Belgium;* G. Meneghesso, *Università degli Studi di Padova, Italy*

13:55 **5-2** **Bidirectional Threshold Voltage Shift and Gate Leakage in 650 V p-GaN AlGaN/GaN HEMTs: The Role of Electron-Trapping and Hole-Injection**
Yuanyuan Shi, Qi Zhou, Qian Cheng, P. Wei, L. Zhu, D. Wei, A. Zhang, Wanjun Chen, Bo Zhang, *University of Electronic Science and Technology of China, China*

14:20 **5-3** **GaN-on-Si Lateral Power Devices with Symmetric Vertical Leakage: The Impact of Floating Substrate**
Hanyuan Zhang, Shu Yang, Kuang Sheng, *Zhejiang University, China*

14:45 **5-4** **Short Circuit Robustness Analysis of New Generation Enhancement-Mode p-GaN Power HEMTs**
M. Riccio, G. Romano, L. Maresca, G. Breglio, A. Irace, *Università degli Studi di Napoli Federico II, Italy;* G. Longobardi, *University of Cambridge, United Kingdom*

15:10 **Coffee Break**
Salon 4-9 (3rd Level)
Tuesday, May 15, 2018

15:30 **Poster Session 6: High Voltage**
Salon 4-9 (3rd Level), Supported by Sinopower Semiconductor.
Tuesday, May 15, 2018
Chair: Tadaharu Minato, *Mitsubishi, Japan*
Co-chair Tom Tsai, *TSMC, Taiwan*

6-1 **Influence of Doping Profiles and Chip Temperature on Short-Circuit Oscillations of IGBTs**
Vera van Treek, Hans-Joachim Schulze, Franz-Josef Niedernostheide, Christian Sandow, Roman Baburske, Frank Pfirsch, *Infineon Technologies AG, Germany*

6-2 **A 750V Recessed-Emitter-Trench IGBT with Recessed-Dummy-Trench Structure Featuring Low Switching Losses**
Yao Yao, Haihui Luo, Qiang Xiao, *Zhuzhou CRRC Times Electric Co., Ltd., China;* Chunlin Zhu, *Dynex Semiconductor Ltd., United Kingdom;* Haibo Xiao, Rongzhen Qin, *Zhuzhou CRRC Times Electric Co., Ltd., China;* Luther-King Ngwendson, *Dynex Semiconductor Ltd., United Kingdom;* Xubin Ning, Canjian Tan, *Zhuzhou CRRC Times Electric Co., Ltd., China;* Ian Deviny, *Dynex Semiconductor Ltd., United Kingdom;* Xiaoping Dai, *Zhuzhou CRRC Times Electric Co., Ltd., China*

6-3 **Small Current Unclamped Inductive Switching (UIS) to Detect Fabrication Defect for Mass-Production Phase IGBT**
Kazuya Sano, Yukio Matsushita, Megumi Yachi, Yoji Nakata, *Mitsubishi Electric Corporation, Japan;* Keiichiro Ide, Daisaku Yoshida, *Kyokuyo Semiconductors Corporation, Japan;* Tomohito Kudo, Yasuo Ata, Hideki Haruguchi, Shinya Soneda, Tadaharu Minato, *Mitsubishi Electric Corporation, Japan*

6-4 **Tailoring the Performance of Silicon Power Diodes by Predictive TCAD Simulation of Platinum**
Moritz Hauf, Christian Sandow, Franz-Josef Niedernostheide, *Infineon Technologies AG, Germany;* Gerhard Schmidt, *Infineon Technologies Austria AG, Austria*

6-5 **Novel 3D Narrow Mesa IGBT Suppressing CIBL**
Masahiro Tanaka, *Nihon Synopsys G.K., Japan;* Akio Nakagawa, *Nakagawa Consulting Office, LLC., Japan*

6-6 **N-Buffer Design Optimization for Short Circuit SOA Ruggedness in 1200V Class IGBT**
Kenji Suzuki, Koichi Nishi, Mitsuru Kaneda, Akihiko Furukawa, *Mitsubishi Electric Corporation, Japan*

6-7 **High Avalanche Capability Specific Diode Part Structure of RC-IGBT based upon CSTBT™**
Shinya Soneda, Shinya Akao, Tetsuo Takahashi, Akihiko Furukawa, *Mitsubishi Electric Corporation, Japan*

6-8 **C_{OSS} Losses in Silicon Superjunction MOSFETs across Constructions and Generations**
Grayson Zulauf, Juan M. Rivas-Davila, *Stanford University, United States*

6-9 **Extending the RET-IGBT (Recessed Emitter Trench IGBT) Concept to High Voltages: Experimental Demonstration of 3.3kV RET IGBT**
L. Ngwendson, I. Deviny, C. Zhu, I. Saddiqui, C. Kong, A. Islam, J. Hutchings, J. Thompson, M. Briggs, O. Basset, *Dynex Semiconductor Ltd., United Kingdom;* H. Luo, Y. Wang, Y. Yao, *Zhuzhou CRRC Times Electric Co., Ltd., China*

6-10 **Temperature Dependence of the On-State Voltage Drop in Field-Stop IGBTs**
L. Maresca, M. Riccio, G. Breglio, A. Irace, *Università degli Studi di Napoli Federico II, Italy;* P. Mirone, C. Sanfilippo, L. Merlin, *Vishay Semiconductor Italiana, Italy*

6-11 **A High-Voltage p-LDMOS with Enhanced Current Capability Comparable to Double RESURF n-LDMOS**
Bo Yi, Junji Cheng, Moufu Kong, Bingke Zhang, Xing Bi Chen, *University of Electronic Science and Technology of China, China*

6-12 **Self Terminating Lateral-Vertical Hybrid Super-Junction FET that Breaks R_{DS}.A – Charge Balance Trade-Off Window**
Karthik Padmanabhan, Lingpeng Guan, Madhur Bobde, Sik Lui, *Alpha and Omega Semiconductor, Inc., United States;* Anup Bhalla, *United Silicon Carbide Inc., United States;* Hamza Yilmaz, *Computime Limited, China;* Lei Zhang, *Jireh Semiconductor, Inc., United States*

6-13 **Local Lifetime Control for Enhanced Ruggedness of HVDC Thyristors**
J. Vobecky, V. Botan, K.U. Meier, K. Tugan, M. Bellini, *ABB Switzerland Ltd., Switzerland*

6-14 **Low Injection Anode as Positive Spiral Improvement for 650V RC-IGBT**
Ryu Kamibaba, Mitsuru Kaneda, Tetsuo Takahashi, Akihiko Furukawa, *Mitsubishi Electric Corporation, Japan*

6-15 **Observation of Current Filaments in IGBTs with Thermoreflectance Microscopy**
Riteshkumar Bhojani, Jens Kowalsky, Josef Lutz, *Technische Universität Chemnitz, Germany;* Dustin Kendig, *Microsanj, United States;* Roman Baburske, Hans-Joachim Schulze, Franz-Josef Niedernostheide, *Infineon Technologies AG, Germany*

6-16 **IGBT Structure with Electrically Separated Floating-P Region improving Turn-On dVak/dt Controllability**
Yoshihiro Ikura, Yuichi Onozawa, *Fuji Electric Co., Ltd., Japan;* Akio Nakagawa, *Nakagawa Consulting Office, LLC., Japan*

6-17 **Optimization of Trench Sidewall for Low Leakage Current of the Sloped Field Plate Trench Edge Termination**
Wentao Yang, *Hong Kong University of Science and Technology, China;* Xianda Zhou, *Hong Kong University of Science and Technology and Sun Yat-sen University, China;* Chao Xiao, Hao Feng, Yong Liu, Xiangming Fang, *Hong Kong University of Science and Technology, China;* Yuichi Onozawa, Hiroyuki Tanaka, Kaname Mitsuzuka, *Fuji Electric Co., Ltd., Japan;* Johnny K.O. Sin, *Hong Kong University of Science and Technology, China*

6-18 **Analysis of Reverse Temperature Dependent Switching-Off Behavior of Ultra-Thin Fieldstop IGBTs**
So-Youn Kim, Euntaek Kim, Jiho Jeon, Jinyoung Jung, Soo-Seong Kim, Kwang-Hoon Oh, Chongman Yun, *TRinno Technology, Korea*

6-19 **Effect of Charge Imbalance and Edge Structure on the Reverse Recovery Waveform in Superjunction Body Diode**
Daisuke Arai, Mizue Yamaji, Koichi Murakami, Masaaki Honda, Shinji Kunori, *Shindengen Electric Manufacturing Co., Ltd., Japan*

6-20 **Tight Relationship among Field Failure Rate, Single Event Burn-Out (SEB) and Cold Bias Stability (CBS) as a Cosmic Ray Endurance for IGBT and Diode**
K. Suzuki, Y. Yoshiura, K. Uryu, T. Minato, M. Tarutani, Y. Miyazaki, H. Uemura, T. Hagihara, S. Momii, Y. Kusakabe, M. Nakamura, *Mitsubishi Electric Corporation, Japan;* Y. Fujita, K. Takakura, *MELCO Semiconductor Engineering Corporation, Japan*

15:30 **Poster Session 7: GaN**
Salon 4-9 (3rd Level), Supported by Sinopower Semiconductor.
Tuesday, May 15, 2018
Chair: Tadaharu Minato, *Mitsubishi, Japan*
Co-chair Tom Tsai, *TSMC, Taiwan*

7-1 **Gate Architecture Design for Enhancement Mode p-GaN Gate HEMTs for 200 and 650V Applications**
N.E. Posthuma, S. You, S. Stoffels, H. Liang, M. Zhao, S. Decoutere, *imec, Belgium*

7-2 **Uni-Directional GaN-on-Si MOSHEMTs with High Reverse-Blocking Voltage based on Nanostructured Schottky Drain**
Jun Ma, Elison Matioli, *École Polytechnique Fédérale de Lausanne, Switzerland*

7-3 **Characterization of GaN-HEMT in Cascode Topology and Comparison with State of the Art-Power Devices**
Sven Buetow, Reinhard Herzer, *Semikron Elektronik GmbH & Co. KG, Germany*

7-4 **Performance Enhancement of CMOS Compatible 600V Rated AlGaN/GaN Schottky Diodes on 200mm Silicon Wafers**
J. Biscarrat, R. Gwoziecki, Y. Baines, J. Buckley, C. Gillot, W. Vandendaele, G. Garnier, M. Charles, M. Plissonnier, *Université Grenoble Alpes, CEA-LETI, France*

7-5 **Novel AlGaN/GaN SBDs with Nanoscale Multi-Channel for Gradient 2DEG Modulation**
Anbang Zhang, Qi Zhou, Chao Yang, Yuanyuan Shi, Changxu Dong, *University of Electronic Science and Technology of China, China;* Tong Liu, *Chinese Academy of Sciences, China;* Yijun Shi, Wanjun Chen, Zhaoji Li, Bo Zhang, *University of Electronic Science and Technology of China, China*

7-6 **Switching Performance Analysis of GaN OG-FET using TCAD Device-Circuit-Integrated Model**
Dong Ji, Wenwen Li, Srabanti Chowdhury, *University of California, Davis, United States*

7-7 **A Split Gate Vertical GaN Power Transistor with Intrinsic Reverse Conduction Capability and Low Gate Charge**
Ruopu Zhu, Qi Zhou, Hong Tao, Yi Yang, Kai Hu, Dong Wei, Liyang Zhu, Yu Shi, Wanjun Chen, Xiaorong Luo, Bo Zhang, *University of Electronic Science and Technology of China, China*

7-8 **Experimental Characterization of the Fully Integrated Si-GaN Cascoded FET**
Jie Ren, Chak Wah Tang, Hao Feng, Huaxing Jiang, Wentao Yang, *Hong Kong University of Science and Technology, China;* Xianda Zhou, *Hong Kong University of Science and Technology and Sun Yat-Sen University, China;* Kei May Lau, Johnny K.O. Sin, *Hong Kong University of Science and Technology, China*

7-9 **Effect of Device Layout on the Switching of Enhancement Mode GaN HEMTs**
Loizos Efthymiou, Gianluca Camuso, Giorgia Longobardi, Florin Udrea, *University of Cambridge, United Kingdom;* Terry Chien, Max Chen, *Vishay General Semiconductor, Taiwan;* Ayman Shibib, Kyle Terrill, *Vishay Siliconix, United States*

7-10 **A Balancing Method for Low R_{on} and High V_{th} Normally-Off GaN MISFET by Preserving a Damage-Free Thin AlGaN Barrier Layer**
Jialin Zhang, Liang He, Liuan Li, Yiqiang Ni, Taotao Que, Zhenxin Liu, Wenjing Wang, Jiexin Zheng, Yanfen Huang, Jia Chen, Xin Gu, Yawen Zhao, Lei He, Zhisheng Wu, Yang Liu, *Sun Yat-sen University, China*

7-11 **Enhancement of Punch-Through Voltage in GaN with Buried P-Type Layer Utilizing Polarization-Induced Doping**
Wenshen Li, Mingda Zhu, Kazuki Nomoto, Zongyang Hu, *Cornell University, United States;* Xiang Gao, *IQE RF LLC, United States;* Manyam Pilla, *Qorvo Inc., United States;* Debdeep Jena, Huili Grace Xing, *Cornell University, United States*

7-12 **P-Gate GaN HEMT Gate-Driver Design for Joint Optimization of Switching Performance, Freewheeling Conduction and Short-Circuit Robustness**
Han Wu, Asad Fayyaz, Alberto Castellazzi, *University of Nottingham, United Kingdom*

7-13 **Monolithic Integration of GaN-Based NMOS Digital Logic Gate Circuits with E-Mode Power GaN MOSHEMTs**
Minghua Zhu, Elison Matioli, *École Polytechnique Fédérale de Lausanne, Switzerland*

7-14 **645 V Quasi-Vertical GaN Power Transistors on Silicon Substrates**
Chao Liu, Riyaz Abdul Khadar, Elison Matioli, *École Polytechnique Fédérale de Lausanne, Switzerland*

15:30 **Poster Session 8: Packaging**
Salon 4-9 (3rd Level), Supported by Sinopower Semiconductor.
Tuesday, May 15, 2018
Chair: Tadaharu Minato, *Mitsubishi, Japan*
Co-chair Tom Tsai, *TSMC, Taiwan*

8-1 **Effects of Inorganic Encapsulation on Power Cycling Lifetime of Aluminum Bond Wires**
Nan Jiang, *Technische Universität Chemnitz, Germany;* Markus G. Scheibel, Benjamin Fabian, Marko Kalajica, Anton-Zoran Miric, *Heraeus Deutschland GmbH & Co. KG, Germany;* Josef Lutz, *Technische Universität Chemnitz, Germany*

8-2 **Sn- and Cu-Oxide Reduction by Formic Acid and its Application to Power Module Soldering**
Naoto Ozawa, Tatsuo Okubo, Jun Matsuda, Tatsuo Sakai, *Origin Electric Co., Ltd., Japan*

8-3 **Dynamic Characterisation and Optimisation of Multiply Contacted Power Busbars**
Vanessa Basler, Andreas Wagner, Wolfgang Hölzl, Gerhard Wachutka, *Technische Universität München, Germany*

8-4 **Development of a Highly Integrated 10 kV SiC MOSFET Power Module with a Direct Jet Impingement Cooling System**
Bassem Mouawad, Robert Skuriat, Jianfeng Li, C. Mark Johnson, *University of Nottingham, United Kingdom;* Christina DiMarino, *Virginia Polytechnic Institute and State University, United States*

8-5 **A More Accurate Electromagnetic Modeling of WBG Power Modules**
Ivana Kovačević-Badstübner, Ulrike Grossner, *ETH Zürich, Switzerland;* Daniele Romano, Giulio Antonini, *Università degli Studi dell'Aquila, Italy;* Jonas Ekman, *Luleå University of Technology, Sweden*

8-6 **Accelerated Thermal Fatigue Test of Metallized Ceramic Substrates for SiC Power Modules by Repeated Four-Point Bending**
Hiroyuki Miyazaki, Hideki Hyuga, Kiyoshi Hirao, Hiroshi Sato, Hiroshi Yamaguchi, *National Institute of Advanced Industrial Science and Technology, Japan;* Shoji Iwakiri, Hideki Hirotsuru, *Denka Co., Ltd., Japan*

8-7 **Dynamic Stability Analysis based on State-Space Model and Lyapunov's Stability Criterion for SiC-MOS and Si-IGBT Switching**
Xiao Zeng, Zehong Li, Yuzhou Wu, Wei Gao, Jinping Zhang, Min Ren, Bo Zhang, *University of Electronic Science and Technology of China, China*

Ad Com Dinner (by invitation only)

18:30 **Tuesday, May 15, 2018**

9. GaN Power Devices - 2

Red Lacquer Room (4th Level)
Wednesday, May 16, 2018
Chair: Peter Moens, *ON Semiconductor, Belgium*
Co-chair Yang Liu, *Sun Yat-sen University, China*

08:30 **9-1** **1 kV/1.3 mΩ cm² Vertical GaN-on-GaN Schottky Barrier Diodes with High Switching Performance**
Shu Yang, Shaowen Han, Rui Li, Kuang Sheng, *Zhejiang University, China*

08:55 **9-2** **Reverse-Blocking AlGaN/GaN Normally-Off MIS-HEMT with Double-Recessed Gated Schottky Drain**
Jiacheng Lei, Jin Wei, Gaofei Tang, Kevin J. Chen, *Hong Kong University of Science and Technology, China*

09:20 **9-3** **Recess-Free AlGaN/GaN Lateral Schottky Barrier Controlled Schottky Rectifier with Low Turn-On Voltage and High Reverse Blocking**
Xuanwu Kang, Xinhua Wang, Sen Huang, Jinhan Zhang, Jie Fan, Shuo Yang, Yuankun Wang, Yingkui Zheng, Ke Wei, Jin Zhi, Xinyu Liu, *Institute of Microelectronics of Chinese Academy of Sciences, China*

09:45 **9-4** **[Late News] An Industry-Ready 200 mm p-GaN E-Mode GaN-on-Si Power Technology**
N.E. Posthuma, S. You, S. Stoffels, D. Wellekens, H. Liang, M. Zhao, B. De Jaeger, K. Geens, N. Ronchi, S. Decoutere, *imec, Belgium;* P. Moens, A. Banerjee, H. Ziad, M. Tack, *ON Semiconductor, Belgium*

10:10 **Coffee Break**
Salon 4-9 (3rd Level)
Wednesday, May 16, 2018

10:10 **Poster Session 10: Low Voltage Technology**
Salon 4-9 (3rd Level), Supported by Sinopower Semiconductor.
Wednesday, May 16, 2018
Chair: David Tsung-Yi Huang, *Richtek, Taiwan*
Co-chair Sameer Pendharkar, *Texas Instruments, USA*

10-1 **Application-Driven Device/Circuit Co-Simulation Framework for Power MOSFET Design and Technology Development**
Tirthajyoti Sarkar, Ashok Challa, Kirk Huang, Prasad Venkatraman, Dean Probst, *ON Semiconductor, United States*

10-2 **A Novel High Performance Medium-Voltage DEnMOS in 40nm CMOS Technology**
Wei Lin, Upinder Singh, Jeoung Mo Koo, Huihua Jiang, *Globalfoundries, Singapore*

10-3 **Novel Current Re-Distribution Structure for Improved and Easy-to-Manufacturing 24V LDMOS**
Cheng-Hua Lin, Yan-Liang Ji, C.H. Jan, C.W. Hu, Keven Chang, H.W. Kao, *MediaTek Inc., Taiwan*

10-4 **A Novel Divided STI-Based nLDMOSFET for Suppressing HCI Degradation under High Gate Bias Stress**
Takahiro Mori, Shunji Kubo, Takashi Ipposhi, *Renesas Semiconductor Manufacturing Co., Ltd., Japan*

10-5 **Hot-Carrier Induced Off-State Leakage Current Increase of LDMOS and Approach to Overcome the Phenomenon**
Keita Takahashi, Kanako Komatsu, Toshihiro Sakamoto, Koji Kimura, Fumitomo Matsuoka, *Toshiba Electronic Devices & Storage Corporation, Japan;* Yoshiaki Ishii, Katsumi Egashira, Masaki Sakai, *Japan Semiconductor Corporation, Japan*

10-6 **Novel Approach for NLDMOS Performance Enhancement by Critical Electric Field Engineering**
Jaroslav Pjenčák, *ON Semiconductor, Czech Republic;* Moshe Agam, *ON Semiconductor, United States;* Ladislav Šeliga, *ON Semiconductor, Czech Republic;* Thierry Yao, Agajan Suwhanov, *ON Semiconductor, United States*

10-7 **A 0.35μm 600V Ultra-Thin Epitaxial BCD Technology for High Voltage Gate Driver IC**
Huihui Wang, *Shanghai Huahong Grace Semiconductor Manufacturing Corporation, China;* Ming Qiao, *University of Electronic Science and Technology of China, China;* Feng Jin, *Shanghai Huahong Grace Semiconductor Manufacturing Corporation, China;* Yang Yu, ZhangYi'an Yuan, *University of Electronic Science and Technology of China, China;* Binbin Miao, Wenqing Yang, Jie Wu, Wensheng Qian, Tong Deng, Donghua Liu, Ziquan Fang, Wenting Duan, Jiye Yang, Weiran Kong, *Shanghai Huahong Grace Semiconductor Manufacturing Corporation, China;* Bo Zhang, *University of Electronic Science and Technology of China, China*

10-8 **Impact of Self-Heating Effect in Hot Carrier Injection Modeling**
Dong Seup Lee, Dhanoop Varghese, Arif Sonnet, Jungwoo Joh, Archana Venugopal, Srikanth Krishnan, *Texas Instruments, United States*

10-9 **Duty-Cycle-Accelerated Hot-Carrier Degradation and Lifetime Evaluation for 700V Lateral DMOS**
Siyang Liu, Zhichao Li, Wangran Wu, Weifeng Sun, *Southeast University, China;* Shulang Ma, Yuwei Liu, Wei Su, Xiaohong Liu, *CSMC Technologies Corporation, China*

10-10 **A High-Speed SOI-LIGBT with Electric Potential Modulation Trench and Low-Doped Buried Layer**
Shaohong Li, Long Zhang, Jing Zhu, Weifeng Sun, Qingxi Tang, Hao Wang, Ling Sun, *Southeast University, China;* Yan Gu, Shikang Cheng, Sen Zhang, *CSMC Technologies Corporation, China;* Yangbo Yi, *Wuxi Chipown Microelectronics Ltd., China*

10-11 **A Comparison of Close-Cell, Stripe-Cell, and Orthogonal-Cell Low Voltage Superjunction Trench Power MOSFETs for Linear Mode Application**
Yi Su, Madhur Bobde, Sik Lui, Hong Chang, *Alpha and Omega Semiconductor, Inc., United States;* Qinhai Jin, Lei Zhang, *Jireh Semiconductor, Inc., United States*

10-12 **A 150V Novel High-Voltage LDMOS in a 0.18um BCD Plug-In Process**
Yen-Ming Chen, Chiu-Ling Lee, Min-Hsuan Tsai, Chiu-Te Lee, Chih-Chong Wang, *United Microelectronics Corporation, Taiwan*

10-13 **Application of CS-MCT in DC Solid State Circuit Breaker (SSCB)**
Wanjun Chen, Hong Tao, Chao Liu, Yawei Liu, Chengfang Liu, Jie Liu, Yijun Shi, Qi Zhou, Zhaoji Li, Bo Zhang, *University of Electronic Science and Technology of China, China*

10-14 **ESD Failure Analysis and Robustness Improvement for Multi-STI-Finger LDMOS used as Output Device**
Ran Ye, Siyang Liu, Zhigang Dai, Hongting Chen, Wangran Wu, Weifeng Sun, Shengli Lu, *Southeast University, China;* Wei Su, Feng Lin, Guipeng Sun, *CSMC Technologies Corporation, China*

10:10 **Poster Session 11: IC Design**
Salon 4-9 (3rd Level), Supported by Sinopower Semiconductor.
Wednesday, May 16, 2018
Chair: David Tsung-Yi Huang, *Richtek, Taiwan*
Co-chair Sameer Pendharkar, *Texas Instruments, USA*

11-1 **Integrated Symmetrical High Voltage Inverter for the Excitation of Touch Sensitive Electroluminescent Devices**
Katrin Hirmer, Muhammad Bilal Saif, Klaus Hofmann, *Technische Universität Darmstadt, Germany*

11-2 **A Power Inductor Integration Technology using a Silicon Interposer for DC-DC Converter Applications**
Yixiao Ding, *Hong Kong University of Science and Technology, China;* Xiangming Fang, *Shenzhen CoilEasy Technologies Limited, China;* Yuan Gao, Yuefei Cai, Xing Qiu, Philip K.T. Mok, S.W. Ricky Lee, Kei May Lau, Johnny K.O. Sin, *Hong Kong University of Science and Technology, China*

11-3 **A New 1200 V HVIC with High Side Edge Trigger in Order to Solve the Latch on Failure by the Negative VS Surge**
Kinam Song, Wonhi Oh, Jinkyu Choi, Seunghyun Hong, Sangmin Park, *ON Semiconductor, Korea*

11-4 **A High-Voltage Half-Bridge Gate Drive Circuit for GaN Devices with High-Speed Low-Power and High-Noise-Immunity Level Shifter**
Xin Ming, Xuan Zhang, Zhi-wen Zhang, Xu-dong Feng, Li Hu, Xia Wang, Gang Wu, Bo Zhang, *University of Electronic Science and Technology of China, China*

11-5 **AC/DC Flyback Controller with UHV Integrated Start-Up Current Source in 180nm HVIC Technology**
Hing Kit Kwan, Bai Yen Nguyen, Wen-Cheng Lin, Xiaoxin Liu, Swapnil Pandey, Saikat Chakraborty, Jongjib Kim, Don Disney, *Globalfoundries, Singapore*

10:10 **Poster Session 12: SiC**
Salon 4-9 (3rd Level), Supported by Sinopower Semiconductor.
Wednesday, May 16, 2018
Chair: David Tsung-Yi Huang, *Richtek, Taiwan*
Co-chair Sameer Pendharkar, *Texas Instruments, USA*

12-1 **Evaluation of Gate Oxide Reliability in 3.3kV 4H-SiC DMOSFET with J-Ramp TDDB Methods**
Masakazu Sagawa, Hiroshi Miki, Yuki Mori, Haruka Shimizu, Akio Shima, *Hitachi Ltd., Japan*

12-2 **Repetitive Surge Current Test of SiC MPS Diode with Load in Bipolar Regime**
Shanmuganathan Palanisamy, Jens Kowalsky, Josef Lutz, *Technische Universität Chemnitz, Germany;* Thomas Basler, Roland Rupp, Jasmin Moazzami-Fallah, *Infineon Technologies AG, Germany*

12-3 **Accumulation Channel vs. Inversion Channel 1.2 kV Rated 4H-SiC Buffered-Gate (BG) MOSFETs: Analysis and Experimental Results**
Kijeong Han, B. Jayant Baliga, *North Carolina State University, United States;* Woongje Sung, *State University of New York Polytechnic Institute, United States*

12-4 **Characterization of 1.2 kV SiC Super-Junction SBD Implemented by Trench and Implantation Technique**
Baozhu Wang, Hengyu Wang, Xueqian Zhong, Shu Yang, Qing Guo, Kuang Sheng, *Zhejiang University, China*

12-5 **Normally-OFF Dual-Gate Ga_2O_3 Planar MOSFET and FinFET with High I_{ON} and BV**
H.Y. Wong, N. Braga, R.V. Mickevicius, *Synopsys, Inc., United States;* F. Ding, *University of California, Berkeley, United States*

12-6 **Analysis of Short-Circuit Break-Down Point in 3.3 kV SiC-MOSFETs**
Kazuki Tani, Jun-ichi Sakano, Akio Shima, *Hitachi Ltd., Japan*

12-7 **Electrical Characterization of 1.2kV SiC MOSFET at Extremely High Junction Temperature**
Jiahui Sun, Hongyi Xu, Shu Yang, Kuang Sheng, *Zhejiang University, China*

12-8 **Methodology for Enhanced Short-Circuit Capability of SiC MOSFETs**
Junjie An, Masaki Namai, Hiroshi Yano, Noriyuki Iwamuro, *University of Tsukuba, Japan;* Yusuke Kobayashi, Shinsuke Harada, *National Institute of Advanced Industrial Science and Technology, Japan*

12-9 **27.5 kV 4H-SiC PiN Diode with Space-Modulated JTE and Carrier Injection Control**
Koji Nakayama, *National Institute of Advanced Industrial Science and Technology, Japan;* Tomonori Mizushima, Kensuke Takenaka, *National Institute of Advanced Industrial Science and Technology and Fuji Electric Co., Ltd., Japan;* Akihiro Koyama, *National Institute of Advanced Industrial Science and Technology and Mitsubishi Electric Corporation, Japan;* Yuji Kiuchi, *National Institute of Advanced Industrial Science and Technology and New Japan Radio Co., Ltd., Japan;* Shinichiro Matsunaga, Hiroyuki Fujisawa, *National Institute of Advanced Industrial Science and Technology and Fuji Electric Co., Ltd., Japan;* Tetsuo Hatakeyama, *National Institute of Advanced Industrial Science and Technology, Japan;* Manabu Takei, *National Institute of Advanced Industrial Science and Technology and Fuji Electric Co., Ltd., Japan;* Yoshiyuki Yonezawa, *National Institute of Advanced Industrial Science and Technology, Japan;* Tsunenobu Kimoto, *Kyoto University, Japan;* Hajime Okumura, *National Institute of Advanced Industrial Science and Technology, Japan*

12-10 **Investigation on Degradation Mechanism and Optimization for SiC Power MOSFETs under Long-Term Short-Circuit Stress**
Jiaxing Wei, Siyang Liu, Jiong Fang, Sheng Li, Ting Li, Weifeng Sun, *Southeast University, China*

12-11 **High Accuracy Large-Signal SPICE Model for Silicon Carbide MOSFET**
Fu-Jen Hsu, Cheng-Tyng Yen, Chien-Chung Hung, Chwan-Ying Lee, Lurng-Shehng Lee, Kuo-Ting Chu, Ya-Fang Li, *Hestia Power Inc., Taiwan*

12-12 **Analysis of Parameters Determining Nominal Dynamic Performance of 1.2 kV SiC Power MOSFETs**
Roger Stark, Ivana Kovačević-Badstübner, Alexander Tsibizov, Bhagyalakshmi Kakarla, Yanrui Ju, Beat Jaeger, Thomas Ziemann, Ulrike Grossner, *ETH Zürich, Switzerland*

12-13 **SiC Trench IGBT with Diode-Clamped p-Shield for Oxide Protection and Enhanced Conductivity Modulation**
Jin Wei, *Innoscience Technology Co., Ltd., China;* Meng Zhang, *Hong Kong Polytechnic University, China;* Huaping Jiang, *Dynex Semiconductor Ltd., United Kingdom;* Suet To, *Hong Kong Polytechnic University, China;* SungHan Kim, Jun-Youn Kim, *Innoscience Technology Co., Ltd., China;* Kevin J. Chen, *Hong Kong University of Science and Technology, China*

12-14 **Surge Current Failure Mechanisms in 4H-SiC JBS Rectifiers**
Edward Van Brunt, Thomas Barbieri, Adam Barkley, James Solovey, Jim Richmond, Brett Hull, *Wolfspeed, A Cree Company, United States*

12-15 **Surge Capability of 1.2kV SiC Diodes with High-Temperature Implantation**
Hongyi Xu, Jiahui Sun, Jingjing Cui, Jiupeng Wu, Hengyu Wang, Shu Yang, Na Ren, Kuang Sheng, *Zhejiang University, China*

12-16 **Ruggedness of 6.5 kV, 30 A SiC MOSFETs in Extreme Transient Conditions**
Ashish Kumar, Sanket Parashar, *North Carolina State University, United States;* Shadi Sabri, Edward Van Brunt, *Wolfspeed, A Cree Company, United States;* Subhashish Bhattacharya, Victor Veliadis, *North Carolina State University, United States*

12-17 **Next Generation 1200V, 3.5mΩ.cm² SiC Planar Gate MOSFET with Excellent HTRB Reliability**
Sauvik Chowdhury, Kevin Matocha, Blake Powell, Gin Sheh, Sujit Banerjee, *Monolith Semiconductor, Inc., United States*

12-18 **Investigation on Single Pulse Avalanche Failure of 900V SiC MOSFETs**
Na Ren, Hao Hu, Kang L. Wang, *University of California, Los Angeles, United States;* Zheng Zuo, Ruigang Li, *AZ Power Inc., United States;* Kuang Sheng, *Zhejiang University, China*

12-19 **Long Term High Temperature Reverse Bias (HTRB) Test on High Voltage SiC-JBS-Diodes**
Felix Hoffmann, *Universität Bremen, Germany;* Andrei Mihaila, Lukas Kranz, *ABB Switzerland Ltd., Switzerland;* Philippe Godignon, *CNM-CSIC, Spain;* Nando Kaminski, *Universität Bremen, Germany*

12:10 **Lunch Break**

Wednesday, May 16, 2018

13. SiC Reliability and Ruggedness

Red Lacquer Room (4th Level)
Wednesday, May 16, 2018
Chair: Kevin Matocha, *Monolith Semiconductor, USA*
Co-chair Yoshiyuki Yonezawa, *AIST, Japan*

13:30 **13-1** **Robustness Improvement of Short-Circuit Capability by SiC Trench-Etched Double-Diffused MOS (TED MOS)**
Naoki Tega, Kazuki Tani, Digh Hisamoto, Akio Shima, *Hitachi Ltd., Japan*

13:55 **13-2** **High-Temperature Validated SiC Power MOSFET Model for Flexible Robustness Analysis of Multi-Chip Structures**
M. Riccio, V. d'Alessandro, G. Romano, L. Maresca, G. Breglio, A. Irace, *Università degli Studi di Napoli Federico II, Italy;* A. Castellazzi, *University of Nottingham, United Kingdom*

14:20 **13-3** **Reliability Investigation with Accelerated Body Diode Current Stress for 3.3 kV 4H-SiC MOSFETs with Various Buffer Epilayer Thickness**
Yuji Ebiike, Takeshi Murakami, Eisuke Suekawa, Shigehisa Yamamoto, Hiroaki Sumitani, Masayuki Imaizumi, Masayoshi Tarutani, *Mitsubishi Electric Corporation, Japan*

14:45 **13-4** **Dynamic Switching and Short Circuit Capability of 6.5kV Silicon Carbide MOSFETs**
L. Knoll, A. Mihaila, L. Kranz, M. Bellini, S. Wirths, E. Bianda, C. Papadopoulos, M. Rahimo, *ABB Switzerland Ltd., Switzerland*

15:10 **Coffee Break**
Salon 4-9 (3rd Level)
Wednesday, May 16, 2018

14. Packaging and Enabling Technologies

Red Lacquer Room (4th Level)
Wednesday, May 16, 2018
Chair: Tomoyuki Miyoshi, *Hitachi, Japan*
Co-chair Alberto Castellazzi, *Nottingham University, UK*

15:30 **14-1** **Improvement of Power Cycling Reliability of 3.3kV Full-SiC Power Modules with Sintered Copper Technology for $T_{j,max}$=175°C**
Kan Yasui, Seiichi Hayakawa, Masato Nakamura, Daisuke Kawase, Takashi Ishigaki, Koji Sasaki, Toshihito Tabata, Toshiaki Morita, *Hitachi Power Semiconductor Device Ltd., Japan;* Masakazu Sagawa, Hiroyuki Matsushima, Toshiyuki Kobayashi, *Hitachi Ltd., Japan*

15:55 **14-2** **Enhanced Breakdown Voltage and Low Inductance of All-SiC Module**
Motohito Hori, Yuichiro Hinata, Katsumi Taniguchi, Yoshinari Ikeda, Tomoyuki Yamazaki, *Fuji Electric Co., Ltd., Japan*

16:20 **14-3** **Dynamic Performance Analysis of a 3.3 kV SiC MOSFET Half-Bridge Module with Parallel Chips and Body-Diode Freewheeling**
Abdallah Hussein, Bassem Mouawad, Alberto Castellazzi, *University of Nottingham, United Kingdom*

16:45 **14-4** **Power Cycling Reliability Results of GaN HEMT Devices**
Jörg Franke, Guang Zeng, Tom Winkler, Josef Lutz, *Technische Universität Chemnitz, Germany*

17:10 **14-5** **Individual Device Active Cooling for Enhanced System-Level Power Density and More Uniform Temperature Distribution**
Y. Zeng, A. Hussein, A. Castellazzi, *University of Nottingham, United Kingdom*

Banquet
Grand Ballroom (4th Level)
18:30 **Wednesday, May 16, 2018**

15. Novel Device Structures

Red Lacquer Room (4th Level)
Thursday, May 17, 2018
Chair: Dev Alok Girdhar, *Intersil, USA*
Co-chair Alexander Hölke, *XFAB, Malaysia*

08:30 **15-1** **Non-Full Depletion Mode and its Experimental Realization of the Lateral Superjunction**
Wentong Zhang, *University of Electronic Science and Technology of China and CSMC Technologies Corporation, China;* Song Pu, Chunlan Lai, Li Ye, *University of Electronic Science and Technology of China, China;* Shikang Cheng, Sen Zhang, Boyong He, *CSMC Technologies Corporation, China;* Zhuo Wang, Xiaorong Luo, Ming Qiao, Zhaoji Li, Bo Zhang, *University of Electronic Science and Technology of China, China*

08:55 **15-2** **Cathode Short Structure to Enhance the Robustness of Bidirectional Power MOSFETs**
Tanuj Saxena, Vishnu Khemka, Moaniss Zitouni, Raghu Gupta, Ganming Qin, *NXP Semiconductors Inc., United States;* Philippe Dupuy, *NXP Semiconductors Inc., France;* Mark Gibson, *NXP Semiconductors Inc., United States*

09:20 **15-3** **40V to 100V NLDMOS Built on Thin BOX SOI with High Energy Capability, State of the Art Rdson/BVdss and Robust Performance**
Yang Hao, Sim Poh Ching, Madelyn Liew, Alexander Hölke, *X-FAB Sarawak Sdn. Bhd., Malaysia;* Uwe Eckoldt, *X-FAB Semiconductor Foundries, Germany;* Martin Pfost, *Technische Universität Dortmund, Germany*

09:45 **15-4** **Novel Integration Techniques of "Recessed" High Voltage Field-Drift MOSFET with HK/MG RMG Technology**
C.P. Hsiung, P.H. Chiang, S.C. Pu, C.L. Wang, C.W. Lu, K.L. Liu, K.K. Chang, C.C. Yang, N.C. Lee, S.Y. Hsiao, W.F. Lee, C.C. Wang, *United Microelectronics Corporation, Taiwan*

10:10 **Coffee Break**
Salon 4-9 (3rd Level)
Thursday, May 17, 2018

16. IGBTs

Red Lacquer Room (4th Level)
Thursday, May 17, 2018
Chair: Thomas Laska, *Infineon Technologies, Germany*
Co-chair Jan Vobecky, *ABB, Switzerland*

10:30 **16-1** **A Novel Carrier Accumulating Structure for 1200V IGBTs without Negative Capacitance and Decreasing Breakdown-Voltage**
Md Tasbir Rahman, Keisuke Kimura, Takeshi Fukami, Masaki Konishi, Tsuyoshi Nishiwaki, Jun Saito, Kimimori Hamada, *Toyota Motor Corporation, Japan*

10:55 **16-2** **Study on the Improved Short-Circuit Behavior of Narrow Mesa Si-IGBTs with Emitter Connected Trenches**
K. Eikyu, A. Sakai, *Renesas Electronics Corp., Japan;* H. Matsuura, Y. Nakazawa, *Renesas Semiconductor Manufacturing Co., Ltd., Japan;* Y. Akiyama, Y. Yamaguchi, *Renesas Electronics Corp., Japan*

11:20 **16-3** **An Advanced Soft Punch through Buffer Design for Thin Wafer IGBTs Targeting Lower Losses and Higher Operating Temperatures up to 200°C**
Elizabeth Buitrago, Athanassios Mesemanolis, Charalampos Papadopoulos, Chiara Corvasce, Jan Vobecky, Munaf Rahimo, *ABB Switzerland Ltd., Switzerland*

11:45 **16-4** **Investigation of the Mechanism of Gate Voltage Oscillation in 1.2kV IGBT under Short Circuit Condition**
Takuo Kikuchi, *Toshiba Corporation, Japan;* Kazutoshi Nakamura, *Toshiba Electronic Devices & Storage Corporation, Japan;* Kazuto Takao, *Toshiba Corporation, Japan*

12:10 **Lunch Break**
Thursday, May 17, 2018

17. Invited & Late News Papers

Red Lacquer Room (4th Level)
Thursday, May 17, 2018
Chair: Olivier Trescases,
Co-chair Alberto Castellazzi, *Nottingham University, UK*

13:30 **17-1** **[Invited] Design of LED Driver ICs for High-Performance Miniaturized Lighting Systems**
Yuan Gao, Lisong Li, Philip K.T. Mok, *Hong Kong University of Science and Technology, China*

13:55 **17-2** **[Invited] High Voltage Capacitive Voltage Conversion**
Randall L. Sandusky, *Helix Semiconductors, United States;* Alexander Hölke, *X-FAB Sarawak Sdn. Bhd., Malaysia*

14:20 **17-3** **[Late News] Chip-Scale Cooling of Power Semiconductor Devices: Fabrication of Jet Impingement Design**
Feng Zhou, Ki Wook Jung, *Toyota Research Institute of North America, United States;* Yuji Fukuoka, *Toyota Motor Corporation, Japan;* Ercan M. Dede, *Toyota Research Institute of North America, United States*

14:45 **17-4** **[Late News] An Innovative Silicon Power Device (i-Si) through Time and Space Control of a Stored Carrier (TASC)**
Mutsuhiro Mori, Tomoyuki Miyoshi, Tomoyasu Furukawa, Yujiro Takeuchi, Yusuke Hotta, Masaki Shiraishi, *Hitachi Ltd., Japan*

15:10 **Closing**
Red Lacquer Room (4th Level)
Thursday, May 17, 2018

TPC Dinner (by invitation only)
18:30 **Thursday, May 17, 2018**

PARTNERSHIP ORGANIZATIONS

GOLD PARTNERS

SILVER PARTNERS

PowerAmerica Institute
930 Main Campus Drive
Suite 200
Raleigh, NC 27606, USA

The PowerAmerica consortium brings together the brightest minds in the wide bandgap (WBG) power semiconductor world. Semiconductor manufacturers and the companies that use power semiconductors in their products are working together to accelerate the adoption of next generation silicon carbide (SiC) and gallium nitride (GaN) power electronics. Our objective is to educate the workforce and reduce the cost and the perceived risk inherent with this new technology. We fulfill our mission with the backing of the U.S. Department of Energy and the engagement of top researchers from industry, academia, and national laboratories.

Applied Materials, Inc.
3050 Bowers Avenue
P.O. Box 58039
Santa Clara, CA 95054, USA

Applied Materials is a leading equipment supplier to the semiconductor, display and PV industries. Our innovations make possible the technology shaping the future by leveraging our core competencies in:

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  We work at the frontiers of physics and materials science, designing systems with exacting precision and unparalleled production volume capacity. We make constant performance improvements to current materials, while researching and developing the next radical materials advancement.
- Customer Engagement
  We are 100% committed to working closely with our customers to identify and solve their high-value problems. We develop differentiated products that improve our customers' device performance and yield.

Shindengen Electric
New-Ohtemachi Bldg.
2-2-1 Ohtemachi, Chiyoda-ku
Tokyo, 100-0004, Japan

Shindengen has developed and provided innumerable power electronics components for over 70 years. Utilizing our three core technologies – Power Devices, Power Supplies, and Module technology we offer vertically integrated power conversion solutions with emphasis on transportation, clean energy, & motor control innovations.

Synopsys, Inc.
690 East Middlefield Road
Mountain View, CA 94043,
USA

Synopsys, a leader in EDA and semiconductor IP, is also growing its leadership in software security and quality solutions. Whether you're an SoC designer creating advanced semiconductors, or a developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products.

Tektronix, Inc.
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Tektronix delivers innovative, precise and easy-to-operate test and measurement solutions that unlock insights and drive discovery. For wide bandgap applications these include both the Keithley 4200A-SCS parameter analyzer and Series 2400 and 2600B Source Measure Unit instruments as well as the unique Tektronix IsoVu system for isolated differential voltage measurements.

Crosslight Software, Inc.
230-3410 Lougheed Hwy
Vancouver, BC, V5M 2A4
Canada
crosslight.com

Crosslight has been a leading provider of TCAD simulation tools since 1995. With a special focus on compound semiconductor devices, such as GaN HEMTs, Crosslight simulation tools have built a solid reputation in the semiconductor industry for their easy convergence and high accuracy.

Everbeing Int'l Corp.
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Hsinchu City, Taiwan 30080
www.probestation.tw

Everbeing is a world leading manufacturer of probe stations and micropositioners based in Taiwan. With 25 years of history, we strive in producing reliable, precise, user-friendly products with affordable prices. Our solutions cater to vast range of applications, which can be tailored to your specific needs.

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FormFactor is a leading provider of essential test and measurement technologies along the full IC life cycle – from characterization, modeling, reliability and design debug, to qualification and production test. Our products and services enable our customers to accelerate profitability by optimizing device performance and advancing yield knowledge.

Jedat, Inc.
HSB Teppozu, 1-1-12,
Minato, Chuo-ku
Tokyo 104-0043 Japan
www.jedat.co.jp/eng/

Jedat is the leading company for EDA software in Japan. Jedat exhibits PowerVolt, a software product which provide DC analysis, Resistance map analysis, Transient Analysis and Electro-thermal analysis. It works layout data only, no netlist required. User optimizes layout pattern at any phase of design.

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MPI Corporation offers complete Test Solutions based on a variety of engineering probe systems, RF probes from 26 to 110 GHz, and RF calibration software QAlibria®. Major products focus on RF and mmW, Device Characterization for modeling and process development, High Power, and many other complex semiconductor test applications.

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Signatone has been providing manual and semi-automatic wafer probing solutions to semiconductor and materials research community worldwide for 50 years. Signatone PowerPro product line encompass ambient and hot/cold probing of SiC, GaN, and silicon power devices up to 20kV, 500A and in the thermal range of -60°C to 300°C.

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Silicon Frontline's R3D is the leading power device analysis tool.

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Sinopower Semiconductor was established by leading Chinese research and industrial organizations in the field of wide-bandgap semiconductor, including Peking University, Sun Yat-sen University, Epilight Technology and Sino Nitride in 2016. The newly-founded company is endeavoring to become a leading GaN epitaxial wafer and GaN device processing technology provider in China.

TESEC, Inc.
1225 W. 190th Street, Suite 325
Gardena, CA 90248, USA
www.tesecinc.com

TESEC has been a global leader in Power Device Testing Technologies for half a century. The TESEC "SpeKtra" series has become the industry benchmark for Power Device production test. The world focus on energy-saving/low-carbon societies continue to drive TESEC to lead advancements in test systems for new high power device technologies such as SiC/GaN.

TowerJazz
20 Shaul Amor Avenue
P.O. Box 619
Migdal Haemek 2310502,
Israel
towerjazz.com

TowerJazz specializes in manufacturing analog ICs for more than 300 customers worldwide in growing markets, offering SiGe, BiCMOS, Power and Mixed-Signal/CMOS, RF CMOS, CMOS image sensor, and MEMS technologies. TowerJazz also offers design enablement and process transfer services and operates seven manufacturing facilities in Israel, the US and Japan.

ISPSD is the premier forum for technical discussions in all areas of power semiconductor devices and power integrated circuits. ISPSD'19 will be held in the city of Shanghai, one of the most cosmopolitan, diverse, dynamic, vibrant and fascinating cities in China.

Topics of interest include but are not limited to:

- **High Voltage Power Devices**: Medium and high voltage Si bipolar devices such as IGBT, thyristors, pn diodes, etc.
- **Low Voltage Power Devices**: Low and medium voltage Si unipolar devices such as discrete or integrated power MOSFETs, SJ type devices, etc.
- **SiC Power Devices**: SiC-based devices, materials, and processing.
- **GaN and other WBG Power Devices**: GaN and other WBG-based devices, materials, and processing.
- **Power ICs**: Process integration, power IC design, Power-Supply-on-a-Chip, etc.
- **Packaging and Module Technologies**: Integrated power modules and packaging technologies (functionality, power density, isolation, reliability, device cooling, temperature endurance, manufacturing, materials, etc.)

Submission requirement:

- **Abstract submission deadline:** November 12, 2018 (www.ispsd2019.com)
- **Author notification:** January 21, 2019
- **Late news submission (limited acceptance):** March 1, 2019
- **Final manuscript submission deadline:** March 15, 2019
- A PDF abstract should be submitted through the website including a single-page text summary in English (500 words maximum) and up to two additional pages of supporting figures.

General Chair:
Prof. Kuang Sheng, Zhejiang University,
Email: shengk@zju.edu.cn

Technical Program Chair:
Prof. Kevin J. Chen, Hong Kong University of Science and Technology,
Email: eekjchen@ust.hk

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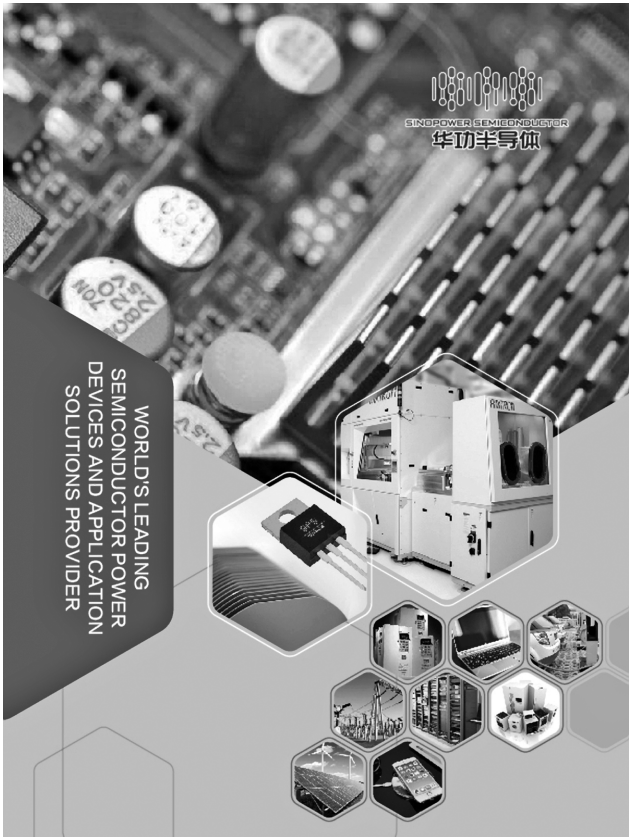

Sinopower Semiconductor Co Ltd("SPS®)is the first enterprise in China specialized in GaN-on-Si wafer and GaN based power devices manufacturing.We offer Gan-on-Si epitaxial wafers ranging in size from 2 inch up to 8 inch GaN power devices, and related application solutions. We provide state-of-the-art products with superior performance and reliability, and are dedicated to become the world 's leading company in the booming wide-bandgap semiconductor industry.

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Vertically Integrated Power Device Manufacturer

With 70 years of experience in the electronics industry, ShinDengen has developed the know-how and experience to provide solutions for innumerable power electronics needs. Utilizing our three core technologies—**Semiconductor Technology**, **Power Circuit Technology**, and **Module Technology**—we are able to serve customers in three central sectors—**Power Devices**, **Car Electronics**, and **Clean Energy Products**. The lineups we provide can be used for a wide variety of uses, and listed below are some of the advantages of using our products to achieve the best possible results.

Diode
- #1 Bridge diode share in the world
- Different uses for many different markets (Automotive, Industrial, Consumer goods, etc.)
- Various product lineups (FRD, SBD, Bridge) and products with 1A~ large current.

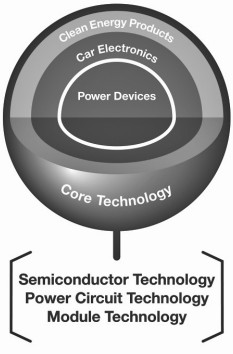
MOSFET
- Ron×Ciss have superior balance levels and thus optimal for motor drive
- Large current lineup from 40V~900V designed by same process which allows for easy selection
- Experience with products such as motors for the automotive industry

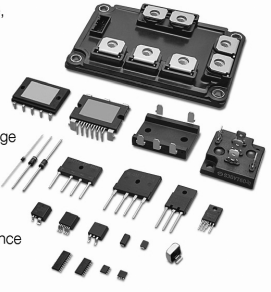
Power Module
- Customizable potting and transfer type modules (most makers only sell standard products)
- Can use Shindengen or other companies die to provide specific solutions
- Experience in multiple industries (Automotive, robotics, industrial, etc.)

Thyristor & TRIAC
- High sensitivity lineup with low noise
- High current surge resistance

TVS
- A variety of products with a large voltage range (VBR 12.5~320V) including SMD types

IC
- High voltage insulated & non-insulated type for LED power supply
- LLC & Quasi-resonance (20 years of experience for a well-developed know-how)
- Standby function allows for extremely low power consumption





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