Updated April 9, 2018

ISPSD 2018 Technical Program

Opening Remarks

Red Lacquer room (4th level)
Monday, May 14, 2018

08:30 John Shen, *Illinois Institute of Technology, USA*

08:50

Plenary 1

Red Lacquer room (4th level)
Monday, May 14, 2018
Chair: John Shen, *Illinois Institute of Technology, USA*
Co-chair K. Sheng, *Zhejiang University, China*

08:50 **PL1-1** **ISPSD: A 30 Year Journey in Advancing Power Semiconductor Technology**
Ayman Shibib, Leo Lorentz, *ECPE, Germany,* Hiromichi Ohashi

09:35 **PL1-2** **Silicon, GaN and SiC: There's Room for All**
Larry Spaziani, *GaN Systems Inc., Canada*

10:20 Coffee Break

Salon 4-9 (3rd level)
Monday, May 14, 2018

Plenary 2

Red Lacquer room (4th level)
Monday, May 14, 2018
Chair: Wai Tung Ng, *Universoty of Toronto, Canada*
Co-chair Kevin Chen, *Hong Kong University of Science and Technology*

10:40 **PL2-1** **Si Wafer Technology for Power Devices: A Review and Future Directions**
Norihisa Machida, *SUMCO, Japan*

11:25 **PL2-2** **The Future of Power Semiconductors: an EU Perspecitve**
Bert De Colvenaer, ECSEL, Belgium

12:10 Lunch Break

Monday, May 14, 2018

1. Superjunction MOS, Diodes and IGBTs

Red Lacquer room (4th level)
Monday, May 14, 2018
Chair: Young Chul Choi, *ON Semiconductor, Korea*
Co-chair Marina Antoniou, *University of Cambridge, UK*

14:00 **1-1** IGBT with Superior Long-Term Switching Behavior by Asymmetric Trench Oxide
Christian Sandow, Philip Brandt, Hans-Peter Felsl, Franz-Josef Niedernostheide, Frank Pfirsch, Francisco Santos, Hans-Joachim Schulze, André Stegner, Frank Umbach, Wolfgang Wagner, *Infineon Technologies AG, Germany*

14:25 **1-2** 6.5 kV Field Shielded Anode (FSA) Diode Concept with 150°C Maximum Operational Temperature Capability
Boni Boksteen, Charalampos Papadopoulos, Daniel Prindle, Arnost Kopta, Chiara Corvasce, *ABB Semiconductors, Switzerland*

14:50 **1-3** Low Noise Superjunction MOSFET with Integrated Snubber Structure
Hiroaki Yamashita, Syotaro Ono, Hisao Ichijo, Masataka Tsuji, Masaru Izumisawa, Wataru Saito, *Toshiba Electronic Devices and Storage Corp., Japan*

15:15 **1-4** Breakthrough of Drain Current Capability and on-Resistance Limits by Gate-Connected Superjunction MOSFET
Wataru Saito, *Toshiba Electric Devices & Storage Corp., Japan*

15:40
Coffee Break
Salon 4-9 (3rd level)
Monday, May 14, 2018

2. SiC Power MOSFETs
Monday, May 14, 2018
Red Lacquer room (4th level)
Chair: Peter Losee, *General Electric, USA*
Co-chair Andrei Petru Mihaila, *ABB, Switzerland*

16:00 **2-1** Investigation of Threshold Voltage Stability of SiC MOSFETs
Dethard Peters, Thomas Aichinger, Thomas Basler, Gerald Rescher, Katja Puschkarsky, Hans Reisinger, *Infineon Technologies AG, Germany*

16:25 **2-2** Deep-P Encapsulated 4H-SiC Trench MOSFETs with Ultra Low $R_{on}Q_{gd}$
Yasuhiro Ebihara, Aiko Ichimura, Shuhei Mitani, Masato Noborio, Yuichi Takeuchi, Shoji Mizuno, Toshimasa Yamamoto, Kazuhiro Tsuruta, *Denso Corp., Japan*

16:50 **2-3** Influence of the Off-State Gate-Source Voltage on the Transient Drain Current Response in SiC MOSFETs
Christian Unger, Martin Pfost, *TU Dortmund University, Germany*

17:15 **2-4** Reduction of RonA Retaining High Threshold Voltage in SiC DioMOS by Improved Channel Design
Atsushi Ohoka, Masao Uchida, Tsutomu Kiyosawa, Yoshihiko Kanzawa, Tetsuzo Ueda, *Automotive & Industrial Systems Co., Panasonic Corp., Japan*

17:40 **2-5** Avalanche Ruggedness and Reverse-Bias Reliability of SiC MOSFET with Integrated Junction Barrier Controlled Schottky Rectifier
Cheng-Tyng Yen, Fu-Jen Hsu, Chien-Chung Hung, Chwan-Ying Lee, Lurng-Shehng Lee, Ya-Fang Li, Kuo-Ting Chu, *Hestia Power Inc., Taiwan*

Reception
Empire room (Lobby Level)
18:15 **Monday, May 14, 2018**

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3. Lateral Devices: Reliability
Red Lacquer room (4th level)
Tuesday, May 15, 2018
Chair: Phil Rutter, *Nexperia, UK*
Co-chair Jun Cai, *Texas instruments, USA*

08:30 **3-1** Comprehensive Investigation on Mechanical Strain Induced Performance Boosts in LDMOS
Wangran Wu, Siyang Liu, Jing Zhu, Weifeng Sun, *Southeast University, China*

08:55 **3-2** Investigation on Total-Ionizing-Dose Radiation Response for High Voltage Ultra-Thin Layer SOI LDMOS

Xin Zhou, Lingfang Zhang, Ming Qiao, Zhangyi'An Yuang, Lei Shu, Ping Luo, Zhaoji Li, Bo Zhang, *University of Electronic Science and Technology of China, China*

09:20 **3-3** Electromigration Current Limit Relaxation for Power Device Interconnects

Jungwoo Joh, Young-Joon Park, Srikanth Krishnan, Kim Christensen, Jayhoon Chung, *Texas Instruments, USA*

09:45 **3-4** Performance and Reliability Insights of Drain Extended FinFET Devices for High Voltage SoC Applications

Sampath Kumar Boeila, Milova Paul, Harald Gossner, Mayank Shrivastava, *Indian Institute of Science, India*

10:10

Coffee Break

Salon 4-9 (3rd level)

Tuesday, May 15, 2018

4. Smart Power ICs

Red Lacquer room (4th level)

Tuesday, May 15, 2018

Chair: Nicolas Rouger, *CNRS, France*

Co-chair Budong (Albert) You, *Silergy Corp., China*

10:30 **4-1** High-Speed, High-Reliability GaN Power Device with Integrated Gate Driver

Gaofei Tang, Alex M.-H. Kwan, R.-Y. Su, F.-W. Yao, Y.-M. Lin, J.-L. Yu, Thomas Yang, Chan-Hong Chern, Tom Tsai, H. C. Tuan, Alexander Kalnitsky, Kevin J. Chen, *The Hong Kong University of Science and Technology, Hong Kong, China*

10:55 **4-2** A 600V High-Side Gate Drive Circuit with Ultra-Low Propagation Delay for Enhancement Mode GaN Devices

Yangyang Lu, Jing Zhu, Weifeng Sun, Yunwu Zhang, Kongsheng Hu, Zhicheng Yu, Jing Leng, Shikang Cheng, Sen Zhang, *Southeast University, China*

11:20 **4-3** A Smart Gate Driver IC for GaN Power Transistors

Jingshu Yu, Weijia Zhang, Andrew Shorten, Rophina Li, Wai Tung Ng, *University of Toronto, Canada*

11:45 **4-4** CMOS Bi-Directional Ultra-Wide-Band Galvanically Isolated Die-to-Die Communication Utilizing A Double-Isolated Transformer

Mahdi Javid, *Arizona State University,* Karel Ptacek, *ON Semiconductor,* Richard Burton, *Atomera Inc.,* Jennifer Kitchen, *Arizona State University, USA*

12:10

Lunch Break

Tuesday, May 15, 2018

5. GaN Power Devices - 1

Red Lacquer room (4th level)

Tuesday, May 15, 2018

Chair: Kevin Chen, *Hong Kong University of Science and Technology, Hong Kong, China*

Co-chair Oliver Haeberlen, *Infineon Technologies, Austria*

13:30 **5-1** Dynamic-R_{on} Control via Proton Irradiation in AlGaN/GaN Transistors

Alaleh Tajalli, Arno Stockman, Matteo Meneghini, Samir Mouhoubi, Abhishek Banerjee, Simone Gerardin, Marta Bagatin, Alessandro Paccagnella, Enrico Zanoni, Marnix Tack, Peter Moens, Gaudenzio Meneghesso, *University of Padova, Italy*

13:55 **5-2** Bidirectional Threshold Voltage Shift and Gate Leakage in 650 V P-GaN AlGaN/GaN HEMTs: the Role of Electron-Trapping and Hole-Injection

Yuanyuan Shi, Qi Zhou, Qian Cheng, Pengcheng Wei, Liyang Zhu, Dong Wei, Anbang Zhang, Wanjun Chen, Bo Zhang, *University of Electronic Science and Technology of China, China*

14:20 **5-3** GaN-on-Si Lateral Power Devices with Symmetric Vertical Leakage: the Impact of Floating Substrate

Hanyuan Zhang, Shu Yang, Kuang Sheng, *Zhejiang University, China*

14:45 **5-4** Short Circuit Robustness Analysis of New Generation Enhancement-Mode pGaN Power HEMTs

Michele Riccio, Gianpaolo Romano, Giorgia Longobardi, Luca Maresca, Giovanni Breglio, Andrea Irace, *University of Naples Federico II, Italy*

15:10

Coffee Break

Salon 4-9 (3rd level)

Tuesday, May 15, 2018

15:30

Poster Session 6: High Voltage

Salon 4-9 (3rd level)

Tuesday, May 15, 2018

Chair: Tadaharu Minato, *Mitsubishi, Japan*

Co-chair Tom Tsai, *TSMC, Taiwan*

6-1 Influence of Doping Profiles and Chip Temperature on Short-Circuit Oscillations of IGBTs

Vera van Treek, Hans-Joachim Schulze, Franz-Josef Niedernostheide, Christian Sandow, Roman Baburske, Frank Pfirsch, *Infineon Technologies AG, Germany*

6-2 A 750V Recessed-Emitter-Trench IGBT with Recessed-Dummy-Trench Structure Featuring Low Switching Losses

Yao Yao, Haihui Luo, Qiang Xiao, Chunlin Zhu, Haibo Xiao, Rongzhen Qin, Luther-King Ngwendson, Xubin Ning, Canjian Tan, Ian Deviny, Xiaoping Dai, *Zhuzhou CRRC Times Electric Co., Ltd., China*

6-3 Small Current Unclamped Inductive Switching (UIS) to Detect Fabrication Defect for Mass-Production Phase IGBT

Kazuya Sano, Shinya Soneda, Tadaharu Minato, *Mitsubishi Electric Corporation, Japan*

6-4 Tailoring the Performance of Silicon Power Diodes by Predictive TCAD Simulation of Platinum

Moritz Hauf, Christian Sandow, Gerhard Schmidt, Franz-Josef Niedernostheide, *Infineon Technologies AG, Germany*

6-5 Novel 3D Narrow Mesa IGBT Suppressing CIBL

Masahiro Tanaka, Akio Nakagawa, *Nihon Synopsys G.K., Japan*

6-6 N-Buffer Design Optimization for Short Circuit SOA Ruggedness in 1200V Class IGBT

Kenji Suzuki, Koichi Nishi, Mitsuru Kaneda, Akihiko Furukawa, *Mitsubishi Electric Corporation, Japan*

6-7 High Avalanche Capability Specific Diode Part Structure of RC-IGBT Based Upon CSTBTTM

Shinya Soneda, Akihiko Furukawa, *Mitsubishi Electric Corporation, Japan*

6-8 A Comparison of Wide-Bandgap and Silicon Power Devices for High- and Very-High-Frequency Soft-Switched Power Converters

Grayson Zulauf, Juan Rivas-Davila, *Stanford University, USA*

6-9 Extending the RET-IGBT (Recessed Emitter Trench IGBT) Concept to High Voltages: Experimental Demonstration of 3.3kV RET IGBT

Luther-King Ngwendson, Ian Deviny, Chunlin Zhu, Chris Kong, Imran Saddiqui, Ariful Islam, Haffee Luoh, Yao Yao, Yangang Wang, John Hutchings, *Dynex Semiconductors, United Kingdom*

6-10 Temperature Dependence of the on-State Voltage Drop in Field-Stop IGBTs

Luca Maresca, Michele Riccio, Giovanni Breglio, Andrea Irace, Paolo Mirone, Carmelo Sanfilippo, Luigi Merlin, *University of Naples - Federico II, Italy*

6-11 A High-Voltage P-LDMOS with Enhanced Current Capability Comparable to Double RESURF N-LDMOS

Bo Yi, Junji Cheng, Moufu Kong, Bingke Zhang, Xingbi Chen, *University of Electronic Science and Technology of China, China*

6-12 Self Terminating Lateral-Vertical Hybrid Super-Junction FET That Breaks Rds.A – Charge Balance Trade-Off Window

Karthik Padmanabhan, Lingpeng Guan, Madhur Bobde, Sik Lui, Anup Bhalla, Hamza Yilmaz, *Alpha and Omega Semiconductor, USA*

6-13 Local Lifetime Control for Enhanced Ruggedness of HVDC Thyristors

Jan Vobecky, Virgliu Botan, Marco Bellini, Urban Meier, Kenan Tugan, *ABB, Switzerland*

6-14 Low Injection Anode As Positive Spiral Improvement for 650V RC-IGBT

Ryu Kamiababa, Mitsuru Kaneda, Tetsuo Takahashi, Akihiko Furukawa, *Mitsubishi Electric Corporation, Japan*

6-15 Observation of Current Filaments in IGBTs with Thermoreflectance Microscopy

Riteshkumar Bhojani, Jens Kowalsky, Dustin Kendig, Josef Lutz, Roman Baburske, Hans-Joachim Schulze, Franz-Josef Niedernostheide, *Technische Universität Chemnitz, Germany*

6-16 A Novel IGBT Structure with High Potential Floating P Region Improving Turn-on dV_{ak}/dt Controllability

Yoshihiro Ikura, Yuichi Onozawa, Akio Nakagawa, *Fuji Electric, Japan*

6-17 Optimization of Trench Sidewall for Low Leakage Current of the Sloped Field Plate Trench Edge Termination

Wentao Yang, Xianda Zhou, Chao Xiao, Hao Feng, Yong Liu, Xiangming Fang, Yuichi Onozawa, Hiroyuki Tanaka, Kaname Mitsuzuka, Johnny K.O. Sin, *The Hong Kong University of Science and Technology, Hong Kong*

6-18 Analysis of Reverse Temperature Dependent Switching-Off Behavior of Ultra-Thin Fieldstop IGBTs

So-Youn Kim, Euntaek Kim, Jiho Jeon, Jinyoung Jung, Soo-Seong Kim, Kwang-Hoon Oh, Chongman Yun, *Trinno Technology, Korea*

6-19 Effect of Charge Imbalance and Edge Structure on the Reverse Recovery Waveform in Superjunction Body Diode

Daisuke Arai, Mizue Yamaji, Koichi Murakami, Masaaki Honda, Shinji Kunori, *Shindengen Electric Manufacturing Co., Ltd., Japan*

6-20 Tight Relationship Among Field Failure Rate, Single Event Burn-Out (SEB) and Cold Bias Stability (CBS) As a Cosmic Ray Endurance for IGBT and Diode

Kenji Suzuki, Yasuhiro Yoshiura, Tadaharu Minato, *Mitsubishi Electric Corporation, Japan*

15:30 Poster Session 7: GaN

Salon 4-9 (3rd level)
Tuesday, May 15, 2018

Chair:	Tadaharu Minato, *Mitsubishi, Japan*
Co-chair	Tom Tsai, *TSMC, Taiwan*
7-1	Gate Architecture Design for Enhancement Mode P-GaN Gate HEMTs for 200 and 650V Applications Niels Posthuma, Shuzhen You, Steve Stoffels, Hu Liang, Ming Zhao, Stefaan Decoutere, *imec, Belgium*
7-2	Uni-Directional GaN-on-Si MOSHEMTs with High Reverse-Blocking Voltage Based on Nanostructured Schottky Drain Jun Ma, Elison Matioli, *École polytechnique fédérale de Lausanne (EPFL), Switzerland*
7-3	Characterization of GaN-HEMT in Cascode Topology and Comparison with State of the Art-Power Devices *Sven Buetow, Reinhard Herzer, Semikron Elektronik GmbH & Co. KG, Germany*
7-4	Performance Enhancement of CMOS Compatible 600V Rated AlGaN/GaN Schottky Diodes on 200mm Silicon Wafers Jerome Biscarrat, Romain Gwoziecki, Yannick Baines, Julien Buckley, Charlotte Gillot, William Vandendaele, Gennie Garnier, Matthew Charles, Marc Plissonnier, *Université Grenoble Alpes, CEA, LETI, France*
7-5	Novel AlGaN/GaN Schottky Barrier Diodes with Comb-Shaped Nanoscale Multi-Channel for Gradient 2DEG Modulation Anbang Zhang, Qi Zhou, Chao Yang, Yuanyuan Shi, Yijun Shi, Wanjun Chen, Zhaoji Li, Bo Zhang, *University of Electronic Science and Technology of China, China*
7-6	Switching Performance Analysis of GaN OG-FET Using TCAD Device-Circuit-Integrated Model Dong Ji, Wenwen Li, Srabanti Chowdhury, *University of California, Davis, USA*
7-7	A Split Gate Vertical GaN Power Transistor with Intrinsic Reverse Conduction Capability and Low Gate Charge Qi Zhou, Ruopu Zhu, Hong Tao, Yi Yang, Kai Hu, Dong Wei, Liyang Zhu, Yu Shi, Wanjun Chen, Bo Zhang, *University of Electronic Science and Technology of China, China*
7-8	Experimental Characterization of the Fully Integrated Si-GaN Cascoded FET *Jie Ren, Chak Wah Tang, Hao Feng, Hua Xing Jiang, Wen Tao Yang, Xian Da Zhou, Kei May Lau, Johnny K.O. Sin, The Hong Kong University of Science and Technology, Hong Kong*
7-9	Effect of Device Layout on the Switching of Enhancement Mode GaN HEMTs Loizos Efthymiou, Gianluca Camuso, Giorgia Longobardi, Terry Chien, Max Chen, Ayman Shibib, Kyle Terrill, Florin Udrea, *University of Cambridge, United Kingdom*
7-10	A Balancing Method for Low Ron and High Vth Normally-Off GaN MISFET by Preserving a Damage-Free Thin AlGaN Barrier Layer *Jialin Zhang, Liang He, Liuan Li, Jiexin Zheng, Zhisheng Wu, Yang Liu,* Sun Yat-sen University, China
7-11	Enhancement of Punch-Through Voltage in GaN with Buried P-Type Layer Utilizing Polarization-Induced Doping Wenshen Li, Mingda Zhu, Kazuki Nomoto, Zongyang Hu, Xiang Gao, Manyam Pilla, Debdeep Jena, Huili Xing, *Cornell University, USA*
7-12	P-Gate GaN HEMT Gate-Driver Design for Joint Optimization of Switching Performance, Freewheeling Conduction and Short-Circuit Robustness Han Wu, Asad Fayyaz, Alberto Castellazzi, *University of Nottingham, United Kingdom*
7-13	Monolithic Integration of GaN-Based NMOS Digital Logic Gate Circuits with E-Mode Power GaN MOSHEMTs

Minghua Zhu, Elison Matioli, *École Polytechnique Fédérale de Lausanne(EPFL), Switzerland*

7-14 First Demonstration of GaN-on-Si Vertical Power MOSFETs
Chao Liu, Riyaz Abdul Khadar, Elison Matioli, *École polytechnique fédérale de Lausanne (EPFL), Switzerland*

15:30

Poster Session 8: Packaging

Salon 4-9 (3rd level)

Tuesday, May 15, 2018

Chair: Tadaharu Minato, *Mitsubishi, Japan*
Co-chair Tom Tsai, *TSMC, Taiwan*

8-1 Effects of Inorganic Encapsulation on Power Cycling Lifetime of Aluminum Bond Wires
Nan Jiang, Markus Scheibel, Benjamin Fabian, Marko Kalajica, Josef Lutz, *Chemnitz University of Technology, Germany*

8-2 Sn- and Cu-Oxide Reduction by Formic Acid and its Application to Power Module Soldering
Naoto Ozawa, Tatsuo Okubo, Jun Matsuda, Tatsuo Sakai, *Origin Electric Co., Ltd., Japan*

8-3 Dynamic Characterisation and Optimisation of Multiply Contacted Power Busbars
Vanessa Basler, Andreas Wagner, Wolfgang Hölzl, Gerhard Wachutka, *Technical University of Munich, Germany*

8-4 Development of a Highly Integrated 10 kV SiC MOSFET Power Module with a Direct Jet Impingement Cooling System
Bassem Mouawad, Christina Dimarino, Robert Skuriat, Jianfeng Li, Christopher Mark Johnson, *University of Nottingham, United Kingdom*

8-5 A More Accurate Electromagnetic Modeling of WBG Power Modules
Ivana Kovacevic-Badstuebner, Daniele Romano, Giulio Antonini, Jonas Ekman, Ulrike Grossner, *Advanced Power Semiconductor Laboratory, ETH Zurich, Switzerland*

8-6 Accelerated Thermal Fatigue Test of Metallized Ceramic Substrates for SiC Power Modules by Repeated Four-Point Bending
Shoji Iwakiri, Hideki Hirotsuru, Hideki Hyuga, Kiyoshi Hirao, Hiroshi Sato, Hiroshi Yamaguchi, *Denka Co., Ltd., Japan*

8-7 Dynamic Stability Analysis Based on State-Space Model and Lyapunov's Stability Criterion for SiC-MOS and Si-IGBT Switching
Xiao Zeng, Zehong Li, Yuzhou Wu, Wei Gao, Jinping Zhang, Min Ren, Bo Zhang, *University of Electronic Science and Technology of China, China*

Ad Com Dinner

18:30 **Tuesday, May 15, 2018**

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9. GaN Power Devices - 2

Red Lacquer room (4th level)

Wednesday, May 16, 2018

Chair: Peter Moens, *ON Semiconductor, Belgium*
Co-chair Yang Liu, *Sun Yat-sen University, China*

08:30 **9-1** 1 kV/1.3 m$\Omega\cdot$cm^2 Vertical GaN-on-GaN Schottky Barrier Diodes with High Switching Performance
Shu Yang, Shaowen Han, Rui Li, Kuang Sheng, *Zhejiang University, China*

08:55 **9-2** Reverse-Blocking AlGaN/GaN Normally-Off Mis-HEMT with Double-Recessed Gated Schottky Drain

Jiacheng Lei, Jin Wei, Gaofei Tang, Kevin J. Chen, *The Hong Kong University of Science and Technology, Hong Kong, China*

09:20 **9-3** Recess-Free AlGaN/GaN Lateral Schottky Barrier Controlled Schottky Rectifier with Low Turn-on Voltage and High Reverse Blocking

Xuanwu Kang, Xinhua Wang, Sen Huang, Jinhan Zhang, Jie Fan, Shuo Yang, Yuankun Wang, Yingkui Zheng, Ke Wei, Xinyu Liu, *IMECAS, China*

09:45 **9-4** An Industry-Ready 200 mm p-GaN E-mode GaN-on-Si power Technology

N.E. Posthuma, S. You, S. Stoffels, D. Wellekens, H. Liang, M. Zhao, B. De Jaeger, K. Geens, N. Ronchi, S. Decoutere, P. Moens, A. Banerjee, H. Ziad, M. Tack, *imec Belgium*

10:10
Coffee Break

Salon 4-9 (3rd level)
Wednesday, May 16, 2018

10:10
Poster Session 10: Low Voltage Technology

Salon 4-9 (3rd level)
Wednesday, May 16, 2018

Chair: David Tsung-Yi Huang, *Richtek, Taiwan*
Co-chair Sameer Pendharkar, *Texas Instruments, USA*

10-1 Application-Driven Device/Circuit co-Simulation Framework for Power MOSFET Design and Technology Development

Tirthajyoti Sarkar, Kirk Huang, Ashok Challa, Prasad Venkatraman, Dean Probst, *ON Semiconductor, USA*

10-2 A Novel High Performance Medium-Voltage DEnMOS in 45nm CMOS Technology

Wei Lin, Upinder Singh, Jeoung Mo Koo, *Globalfoundries Semiconductor Cop., Singapore*

10-3 Novel Current Re-Distribution Structure for Improved and Easy-to-Manufacturing 24V LDMOS

Cheng-Hua Lin, Yan-Liang Ji, Ch Jan, Cw Hu, Keven Chang, HW Kao, *Mediatek Inc., Taiwan*

10-4 A Novel Divided STI-Based nLDMOSFET for Suppressing HCI Degradation Under High Gate Bias Stress

Takahiro Mori, Shunji Kubo, Takashi Ipposhi, *Renesas Semiconductor Manufacturing Co., Ltd. Japan*

10-5 Hot-Carrier Induced Off-State Leakage Current Increase of LDMOS and Approach to Overcome the Phenomenon

Keita Takahashi, Kanako Komatsu, Toshihiro Sakamoto, Koji Kimura, Fumitomo Matsuoka, *Toshiba Electronic Devices & Storage Corporation, Japan*

10-6 Novel Approach for NLDMOS Performance Enhancement by Critical Electric Field Engineering

Jaroslav Pjencak, Moshe Agam, Ladislav Seliga, Thierry Yao, Agajan Suwhanov, *ON Semiconductor, USA*

10-7 A 0.35μm 600V Ultra-Thin Epitaxial BCD Technology for High Voltage Gate Driver IC

Huihui Wang, Ming Qiao, Yang Yu, Zhangyi’an Yuan, Feng Jin, Binbin Miao, Wenqing Yang, Bo Zhang, Wenting Duan, Wensheng Qian, Donghua Liu, Ziquan Fang, *Shanghai Huahong Grace Semiconductor Manufacturing Corporation, China*

10-8 Impact of Self-Heating Effect in Hot Carrier Injection Modeling
Dong Seup Lee, Dhanoop Varghese, Arif Sonnet, Jungwoo Joh, Archana Venugopal , Srikanth Krishnan, Texas Instruments, USA

10-9 Duty-Cycle-Accelerated Hot-Carrier Degradation and Lifetime Evaluation for 700V Lateral DMOS Transistor
Siyang Liu, Zhichao Li, Yunchao Fang, Wangran Wu, Weifeng Sun, Shulang Ma , Yuwei Liu, Wei Su, *Southeast University, China*

10-10 A High-Speed SOI-LIGBT with Electric Potential Modulation Trench and Low-Doped Buried-Layer
Shaohong Li, Long Zhang, Jing Zhu, Weifeng Sun, Qingxi Tang, Hao Wang , Ling , Yan Gu, Shikang Cheng, Sen Zhang, *Southeast University, China*

10-11 A Comparison of Close-Cell, Stripe-Cell and Orthogonal-Cell Low Voltage superjunction Trench Power MOSFETs for Linear Mode Application
Yi Su, Madhur Bobde, Sik Lui, Hong Chang, Qinhai Jin, Lei Zhang, *Alpha and Omega Semiconductor Inc., USA*

10-12 A 150V Novel High-Voltage LDMOS in a 0.18um BCD Plug-In Process
Yen-Ming Chen, Chiu-Ling Lee, Min-Hsuan Tsai, Chiu-Te Lee, Chih-Chong Wang, *United Microelectronics Corporation, Taiwan*

10-13 Application of Cs-MCT in DC Solid State Circuit Breaker (SSCB)
Wanjun Chen, Hong Tao, Chao Liu, Yawei Liu, Chengfang Liu, Jie Liu, Yijun Shi, Qi Zhou, Bo Zhang, *University of Electronic Science and Technology of China, China*

10-14 ESD Failure Analysis and Robustness Improvement for Multi-STI-Finger LDMOS Used As Output Device
Ran Ye, Siyang Liu, Zhigang Dai, Hongting Chen, Wangran Wu, Weifeng Sun, Wei Su, Feng Lin, *Southeast University, China*

10:10

Poster Session 11: IC Design

Wednesday, May 16, 2018
Salon 4-9 (3rd level)
Chair: David Tsung-Yi Huang, *Richtek, Taiwan*
Co-chair Sameer Pendharkar, *Texas Instruments, USA*

11-1 Integrated Symmetrical High-Voltage Inverter for the Excitation of Touch Sensitive Electroluminescent Devices
Katrin Hirmer, Muhammad Bilal Saif, Klaus Hofmann, *TU Darmstadt, Germany*

11-2 A Power Inductor Integration Technology Using a Silicon Interposer for DC-DC Converter Applications
Yixiao Ding, Xiangming Fang, Yuan Gao, Yuefei Cai, Xing Qiu, Philip K.T Mok, S. W. Ricky Lee, Kei May Lau, Johnny K. O Sin, *The Hong Kong University of Science and Technology, Hong Kong*

11-3 A New 1200V HVIC with High Side Edge Trigger in Order to Solve the Latch on Failure by the Negative vs. Surge
Kinam Song, Wonhi Oh, Jinkyu Choi, Seunghyun Hong, Sangmin Park, *ON Semiconductor, Korea*

11-4 A High-Voltage Half-Bridge Gate Drive Circuit for GaN Devices with High-Speed Low-Power and High-Noise-Immunity Level Shifter
Xin Ming, Xuan Zhang, Zhi-Wen Zhang, Xu-Dong Feng, Li Hu, Xia Wang, Gang Wu, Bo Zhang, *University of Electronic Science and Technology of China, China*

11-5 AC/DC Flyback Controller with 700V Integrated Start-Up Current Source in 180nm HVIC Technology

Hing Kit Kwan, Bai Yen Nguyen, Wen-Cheng Lin, Xiaoxin Liu, Swapnil Pandey, Jong Jib , Don Disney, Globalfoundries, Singapore

10:10 Poster Session 12: SiC

Salon 4-9 (3rd level)
Wednesday, May 16, 2018
Chair: David Tsung-Yi Huang, *Richtek, Taiwan*
Co-chair Sameer Pendharkar, *Texas Instruments, USA*

12-1 Evaluation of Gate Oxide Reliability in 3.3kV 4H-SiC DMOSFET with J-Ramp TDDB Methods
Masakazu Sagawa, Hiroshi Miki, Yuki Mori, Haruka Shimizu, Akio Shima, *Hitachi Ltd., Japan*

12-2 Repetitive Surge Current Test of SiC MPS Diode with Load in Bipolar Regime
Shanmuganathan Palanisamy, Jens Kowalsky, Josef Lutz, Thomas Basler, Roland Rupp, *TU Chemnitz, Germany*

12-3 Accumulation Channel Vs. Inversion Channel 1.2 kV Rated 4H-SiC Buffered-Gate (BG) MOSFETs: Analysis and Experimental Results
Kijeong Han, B. Jayant Baliga, Woongje Sung, *North Carolina State University, USA*

12-4 Characterization of 1.2kV SiC Super-Junction SBD Implemented by Trench and Implantation Technique
Baozhu Wang, Hengyu Wang, Xueqian Zhong, Shu Yang, Qing Guo, Kuang Sheng, *Zhejiang University, China*

12-5 Normally-Off Dual-Gate Ga2O3 Planar MOSFET and FinFET with High Current and Breakdown Voltage
Hiu Yung Wong, Fei Ding, Nelson Braga, R. V. Mickevicius, *Synopsys Inc., USA*

12-6 Analysis of Short-Circuit Break-Down Point in 3.3 kV SiC-MOSFETs
Kazuki Tani, Jun-Ichi Sakano, Akio Shima, *Hitachi, Ltd., Japan*

12-7 Electrical Characterization of 1.2kV SiC MOSFET at Extremely High Junction Temperature
Jiahui Sun, Hongyi Xu, Shu Yang, Kuang Sheng, *Zhejiang University, China*

12-8 Methodology for Enhanced Short-Circuit Capability of SiC MOSFETs
Junjie An, Masaki Namai, Yusuke Kobayashi, Hiroshi Yano, Shinsuke Harada, Noriyuki Iwamuro, *University of Tsukuba, Japan*

12-9 27.5 kV 4H-SiC Pin Diode with Space Modulated JTE and Carrier Injection Control
Koji Nakayama, Akihiro Koyama, Yuji Kiuchi, Tetsuo Hatakeyama, Yoshiyuki Yonezawa, Tsunenobu Kimoto, Hajime Okumura, *National Institute of Advanced Industrial Science and Technology (AIST), Japan*

12-10 Investigation on Degradation Mechanism and Optimization for SiC Power MOSFETs Under Long-Term Short-Circuit Shock
Jiaxing Wei, Siyang Liu, Sheng Li, Ting Li, Jiong Fang, Weifeng Sun, *Southeast University, China*

12-11 High Accuracy Large-Signal SPICE Model for Silicon Carbide MOSFET
Fu-Jen Hsu, Cheng-Tyng Yen, Chien-Chung Hung, Chwan-Ying Lee, Lurng-Shehng Lee, Kuo-Ting Chu, Ya-Fang Li, *Hestia Power Inc., Taiwan*

12-12 Analysis of MOSFET Parameters Determining Nominal Dynamic Performance of 1.2 kV SiC Power MOSFETs
Bhagyalakshmi Kakarla, Ivana Kovacevic-Badstuebner, Beat Jaeger, Roger Stark, Thomas Ziemann, Yanrui Ju, Ulrike Grossner, *Advanced Power Semiconductor Laboratory, ETH Zurich, Switzerland*

12-13 SiC Trench IGBT with Diode-Clamped P-Shield for Oxide Protection and Enhanced Conductivity Modulation
Jin Wei, Meng Zhang, Huaping Jiang, Suet To, Sunghan Kim, Junyoun Kim, Kevin J. Chen, *Innoscience Technology Co., Ltd., China*

12-14 Surge Current Failure Mechanisms in 4H-SiC JBS Rectifiers
Edward Van Brunt, Thomas Barbieri, Adam Barkley, James Solovey, Robert Zenoz, Jim Richmond, Brett Hull, *Wolfspeed, A Cree Company, USA*

12-15 Surge Capability of 1.2kV SiC Diode Fabricated with High Temperature Implantation
Hongyi Xu, Jiahui Sun, Jiupeng Wu, Hengyu Wang, Shu Yang, Kuang Sheng, *Zhejiang University, China*

12-16 Ruggedness of 6.5kV, 30A 4H-SiC MOSFETs in Extreme Transient Conditions
Sanket Parashar, Ashish Kumar, Shadi Sabri, Edward Vanbrunt, Subhashish Bhattacharya, Victor Veliadis, *North Carolina State University, USA*

12-17 Next Generation 1200V, 3.5mΩ.cm2 SiC Planar Gate MOSFET with Excellent HTRB Reliability
Sauvik Chowdhury, Kevin Matocha, Blake Powell, Gin Sheh, Sujit Banerjee, *Monolith Semiconductor, USA*

12-18 Investigation on Single Pulse Avalanche Failure of 900V SiC MOSFETs
Na Ren, Hao Hu, Xiaofeng Lyu, Kang L. Wang, Kuang Sheng, *University of California, Los Angeles, USA*

12-19 Long Term High Temperature Reverse Bias (HTRB) Test on High Voltage SiC JBS Diodes
Felix Hoffmann, Andrei Mihaila, Lukas Kranz, Philippe Godignon, Nando Kaminski, *IALB, University of Bremen, Germany*

12:10 Lunch Break

Wednesday, May 16, 2018

13. SiC Reliability and Ruggedness

Red Lacquer room (4th level)
Wednesday, May 16, 2018
Chair: Kevin Matocha, *Monolith Semiconductor, USA*
Co-chair Yoshiyuki Yonezawa, *AIST, Japan*

13:30 **13-1** Robustness Improvement of Short-Circuit Capability by SiC Trench-Etched Double-Diffused MOS (Ted MOS)
Naoki Tega, Kazuki Tani, Digh Hisamoto, Akio Shima, *Hitachi Ltd. Japan*

13:55 **13-2** High-Temperature Validated SiC Power MOSFET Model for Flexible Robustness Analysis of Multi-Chip Structures
Michele Riccio, Vincenzo D'Alessandro, Gianpaolo Romano, Alberto Castellazzi, Luca Maresca, Giovanni Breglio, Andrea Irace, *University of Naples Federico II, Italy*

14:20 **13-3** Reliability Investigation with Accelerated Body Diode Current Stress for 3.3 kV 4H-SiC MOSFETs with Various Buffer Layer Thickness
Yuji Ebiike, *Mitsubishi Electric Corporation, Japan*

14:45 **13-4** Dynamic Switching and Short Circuit Capability of 6.5kV Silicon Carbide MOSFETs
Lars Knoll, Andrei Mihaila, Enea Bianda, Lukas Kranz, Marco Bellini, Stephan Wirths, Charalampos Papadopoulus, *ABB Switzerland Corporate Research, Switzerland*

15:10 Coffee Break

Salon 4-9 (3rd level)

Wednesday, May 16, 2018

14. Packaging and Enabling Technologies

Red Lacquer room (4th level)

Wednesday, May 16, 2018

Chair: Tomoyuki Miyoshi, *Hitachi, Japan*
Co-chair Alberto Castellazzi, *Nottingham University, UK*

15:30 **14-1** Improvement of Power Cycling Reliability of 3.3kV Full-SiC Power Modules with Sintered Copper Technology for $T_{j,max}$=175˚C

Kan Yasui, Seiichi Hayakawa, Masato Nakamura, Daisuke Kawase, Takashi Ishigaki, Kouji Sasaki, Toshihito Tabata, Masakazu Sagawa, Hiroyuki Matsushima, Toshiyuki Kobayashi, Toshiaki Morita, *Hitachi Power Semiconductor Device Ltd., Japan*

15:55 **14-2** Enhanced Breakdown Voltage and Low Inductance of All-SiC Module

Motohito Hori, Yuichiro Hinata, Katsumi Taniguchi, Yoshinari Ikeda, Tomoyuki Yamazaki, *Fuji Electric Co. Ltd., Japan*

16:20 **14-3** Dynamic Performance Analysis of a 3.3 kV SiC MOSFET Half-Bridge Module with Parallel Chips and Body-Diode Freewheeling

Abdallah Hussein, Bassem Mouawad, Alberto Castellazzi, *University of Nottingham, UK*

16:45 **14-4** Power Cycling Reliability Results of GaN HEMT Devices

Jörg Franke, Tom Winkler, Josef Lutz, *Chemnitz University of Technology, Germany*

17:10 **14-5** Individual Device Active Cooling for Enhanced System-Level Power Density and More Uniform Temperature Distribution

Yuqi Zeng, Abdallah Hussein, Alberto Castellazzi, *University of Nottingham, UK*

Banquet

Grand Ballroom (4th level)

18:30 **Wednesday, May 16, 2018**

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15. Novel Device Structures

Red Lacquer room (4th level)

Thursday, May 17, 2018

Chair: Dev Alok Girdhar, *Intersil, USA*
Co-chair Alexander Hölke, *XFAB, Malaysia*

08:30 **15-1** Non-Full Depletion Mode of the Lateral Superjunction and its Experimental Realization in the SOI Devices

Wentong Zhang, Song Pu, Chunlan Lai, Li Ye, Shikang Cheng, Sen Zhang, Boyong He, Zhuo Wang, Xiaorong Luo, Zhaoji Li, Ming Qiao, Bo Zhang, *University of Electronic Science and Technology of China, China*

08:55 **15-2** Cathode Short Structure to Enhance the Robustness of Bidirectional Power MOSFETs

Tanuj Saxena, Vishnu Khemka, Moaniss Zitouni, Raghu Gupta, Ganming Qin, Philippe Dupuy, Mark Gibson, *NXP Semiconductor Inc., USA*

09:20 **15-3** 40V to 100V NLDMOS Built on Thin Box SOI with High Energy Capability, State of the Art R_{dson}/BV_{dss} and Robust Performance

Hao Yang, Martin Pfost, Poh Ching Sim, Madelyn Liew, Alexander Hoelke, Uwe Eckoldt, *X-FAB Semiconductor Foundries AG, Germany*

09:45 **15-4** Novel Integration Techniques of “Recessed” High Voltage Field-Drift MOSFET with HK/MG RMG Technology

Chang Po Hsiung, Ping Hung Chiang, Shih Chieh Pu, Chia Ling Wang, Chia Wen Lu, Kuan Liang Liu, Kai Kuen Chang, Ching Chung Yang, Nien Chung Lee, Shih Yin Hsiao, Wen Fang Lee, Chih Chong Wang*, United Microelectronics Corporation (UMC), Taiwan*

10:10 Coffee Break

Salon 4-9 (3rd level)

Thursday, May 17, 2018

16. IGBTs

Red Lacquer room (4th level)

Thursday, May 17, 2018

Chair: Thomas Laska, *Infineon Technologies, Germany*
Co-chair Jan Vobecky, *ABB, Switzerland*

10:30 **16-1** A Novel Carrier Accumulating Structure for 1200V IGBTs Without Negative Capacitance and Decreasing Breakdown-Voltage

Md Tasbir Rahman, Keisuke Kimura, Takeshi Fukami, Yasuki Futamura, Kimimori Hamada, *Toyota Motor Corporation, Japan*

10:55 **16-2** Study on the Improved Short-Circuit Behavior of Narrow Mesa Si-IGBTs with Emitter Connected Trenches

Katsumi Eikyu, Atsushi Sakai, Hitoshi Matsuura, Yoshito Nakazawa, Yutaka Akiyama, Yasuo Yamaguchi, *Renesas Electronics Corp., Japan*

11:20 **16-3** An Advanced Soft Punch Through Buffer Design for Thin Wafer IGBTs Targeting Lower Losses and Higher Operating Temperatures Up to 200°C

Elizabeth Buitrago, Athanassios Mesemanolis, Charalampos Papadopoulos, Chiara Corvasce, Jan Vobecky, Munaf Rahimo, *ABB Semiconductor, Switzerland*

11:45 **16-4** Investigation of the Mechanism of Gate Voltage Oscillation in 1.2kV IGBT Under Short Circuit Condition

Takuo Kikuchi, Kazutoshi Nakamura, Kazuto Takao, *Toshiba Corporation, Japan*

12:10 Lunch Break

Thursday, May 17, 2018

17. Invited Papers

Red Lacquer room (4th level)

Thursday, May 17, 2018

Chair: Olivier Trescases,
Co-chair Alberto Castellazzi, *Nottingham University, UK*

13:30 **17-1** Design of LED Driver ICs for High- Performance Miniaturized Lighting Systems

P.K.T. Mok, *The Hong Kong University of Science and Technology, Hong Kong, China*

17:55 **17-2** High Voltage Capacitive Voltage Conversion

Randall L. Sandusky, *Helix Semiconductors, USA*

14:20 **17-3** Chip-Scale Cooling of Power Semiconductor Devices

Feng Zhou, Ki Wook Jung, Yuji Fukuoka, Ercan M. Dede, *Toyota Research Institute of North America, USA*

14:45 **17-4** An Innovated Silicon Power Device (i-Si) through Time and Space Control of a Stored Carrier (TASCs)

Mutsuhiro Mori, Tomoyuki Miyoshi, Tomoyasu Furukawa, Yujiro Takeuchi, Yusuke Hotta, Masaki Shiraishi, *Hitachi, Ltd., Japan*

15:10

Closing

Red Lacquer room (4th level)
Thursday, May 17, 2018

TPC Dinner

18:30 **Thursday, May 17, 2018**