Advances in Silicon Power Semiconductor Device Technology with Charge Balance

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Abstract

Silicon power MOSFETs have made tremendous advancements in the past decade. The key concept that has led to this is that of charge balance. In conventional power MOSFET device the maximum doping level and the thickness of the drift region is limited by blocking voltage constraints and a triangular electric field results in its sub-optimal utilization.

The concept of charge balance involves adding an opposite polarity of charge in the drift region compared to default doping to modify the shape of electric field from triangular to trapezoidal for better utilization of drift region for voltage blocking and allow significantly higher doping concentration for lower conduction losses. For low voltages (below 400V) the popular device structure to achieve this is the Split Gate Transistor (SGT). This device utilizes trench MOS charge balance with a shield electrode under the gate. In addition to significantly improving the On Resistance per unit area (~3x for 100V blocking), the shield electrode also significantly reduced the gate to drain miller capacitance (Crss) and Crss/Ciss ratio to allow for high frequency switching.

For high voltages above 400V, the depth of trench and thickness of liner oxide make SGT device impractical to fabricate. As a result, the Super-Junction transistor has emerged as the most successful MOSFET for high voltages. This device utilizes alternating P and N columns in the drift region thereby creating a charge balance. Methods such as multi epi, deep trench and fill have been demonstrated and are commercially successful for making superjunction transistors. These can achieve an On-Resistance reduction of up to 8x compared to planar DMOS transistor. However, presence of alternating P and N columns also results in peculiar Capacitance curves, particularly the Crss which drops sharply at low drain biases and then increases at higher drain biases. It also exhibits snappy diode reverse recovery.

Charge balanced structure is also finding use in bipolar devices such as IGBT and Fast recovery diodes. In these devices, charge balance is used for various performance enhancements such as improving turn-off losses, injection enhancement, and controlling injection efficiency for faster switching.

The goal of this seminar is to understand the device physics and electrical characteristics of charge balanced devices in unipolar and bipolar power devices. This seminar is intended for intermediate level audience.

Biography

Dr. Madhur Bobde received his Bachelors and Masters degree (Integrated) from the Indian Institute of Technology, Bombay, India in 1997 and his PhD. from North Carolina State University in 2000. His PhD. Field of study was Accumulation channel devices (ACCUFETs and ACBTs).

He is currently employed with Alpha & Omega Semiconductor as Vice President of Device Technology. His research areas include high Voltage IGBTs and Fast Recover Diodes; Charge balanced HV MOSFETs & Split Gate transistor for Low Voltage & Fast switching applications and Transient Voltage Suppressors. Prior to that, Madhur was employed with Intel Corporation, where he was involved with the development of design methodology of Static RAM and Content Addressable Memory Cells for 3 generations of Pentium Microprocessors.

He holds more than 100 US granted patents with several pending in this field, and has many publications in premier power conferences such as ISPSD (International Symposium on Power Semiconductor Devices) and APEC (Applied Power Electronics Conference). He is also a Technical Committee member of ISPSD.

Topic Outline

1. Introduction to Power Semiconductor Devices
    a. Device Structure of Planar & Trench MOSFETs
    b. Components of On Resistance
    c. Drift region design trade-offs and Optimization
    d. Capacitances and switching performance
    e. UIS and Diode Reverse Recovery Robustness

2. Concept of Charge Balance
    a. Trench MOS
        i. Device Structure
        ii. Impact on the shape of electric field & blocking capability
        iii. Optimum doping profile
        iv. Requirements on Trench depth and oxide thickness
    b. Superjunction
        i. Device Structure
        ii. Impact on the shape of electric field & blocking capability
        iii. Optimum doping profile & upper limit
        iv. Impact of Charge imbalance on electrical characteristics
3. Split Gate Transistors
    a. Device Structure(s) & Operation
        i. Forward blocking
        ii. Conduction
        iii. Switching
        iv. Diode Reverse Recovery
        v. Hot carrier Injection & Avalanche Robustness
    b. Device fabrication and scaling trends
    c. SGT typical applications
        i. High frequency DC-DC converter Applications
        ii. Secondary Synchronous Rectification

4. Super Junction Transistors
    a. Device Structure(s) & Operation
        i. Forward blocking
        ii. Conduction
        iii. Capacitance curves characteristics
        iv. Switching
        v. Diode Reverse Recovery
        vi. Avalanche Robustness
    b. Device fabrication and scaling trends
    c. Superjunction typical applications

i. PFC & Flyback converters
ii. LLC & Motor Drive

5. Charge Balance in IGBT and Fast Recovery Diodes
    a. Super Junction IGBT
        i. Device Structure & Operation
        ii. Impact of P column on Turn off
        iii. Performance improvement & fabrication complexity trade-off
    b. Trench MOS for Injection Enhancement
        i. TSPG-IGBT Device structure
        ii. Injection Enhancement with Trench MOS
        iii. Performance improvement (Conduction losses, short circuit SOA)
    c. TMBS Diodes
        i. Device Structure & Operation
        ii. Performance improvement (Leakage and Conduction losses)
    d. Injection Efficiency controlled Diodes
        i. Device Structure & Operation
        ii. Performance improvement (Leakage and Conduction losses)